CS4332BSE

High Performance Two-Channel Audio DAC

Features

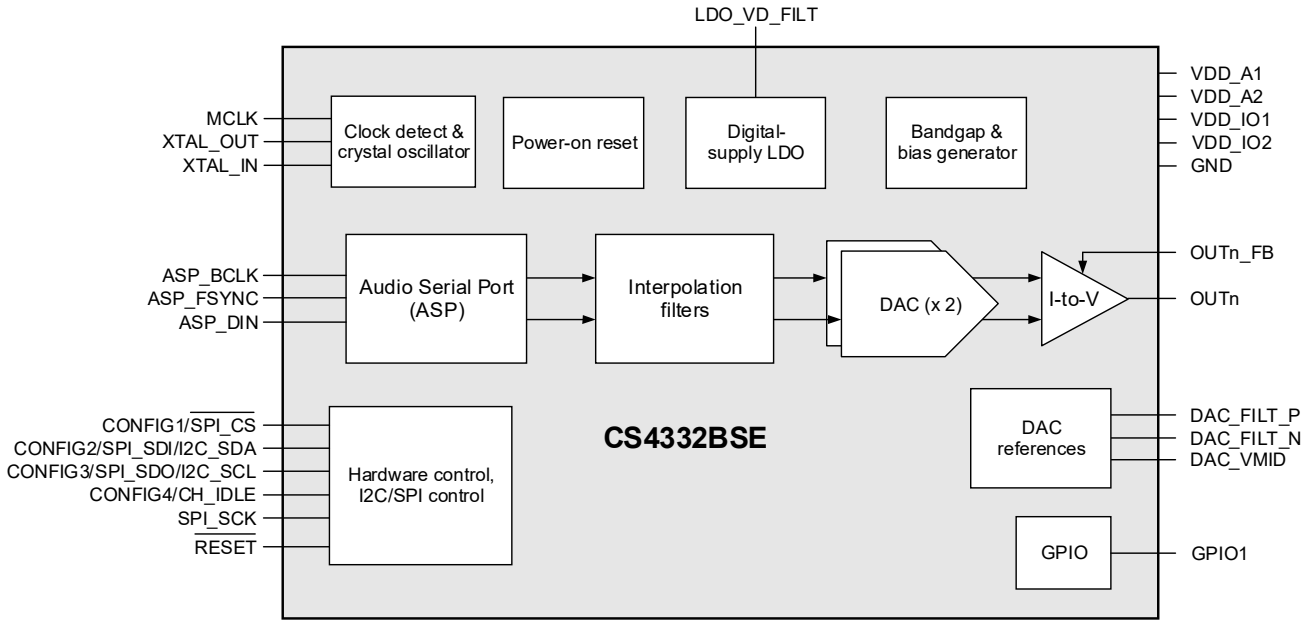
- High performance two-channel DAC
  - Single-ended analog architecture
  - High-resolution 32-bit digital design
  - Low-latency digital filters and digital volume control
- Crystal oscillator interface
- Sample timing alignment across multiple devices
- Signal-activity detection
- Audio serial port (ASP) sample rates up to 384 kHz
  - I^2S, left-justified, and TDM data formats
- Hardware and software control modes
  - I^2C control port up to 1 MHz
  - SPI control port up to 24 MHz
  - Hardware control with no host processor required
- Single-supply operation at 3.3 V
  - Support for 1.8 V–3.3 V digital input/output
  - 40-pin QFN package

Specifications

- Enhanced oversampling sigma-delta voltage-output DAC
  - 115 dB dynamic range (A-weighted)
  - –102 dB total harmonic distortion + noise (THD+N)
  - 4.6/Fs group delay at 48 kHz sample rate
  - 1 V_{RMS} full-scale output

Applications

- A/V receivers
- Digital mixing consoles
- Powered speakers
- Power amplifiers
- High-performance speakers and soundbars
- DAW interfaces
- Musical instruments
- Commercial audio systems



Advanced Product Information

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General Description

The CS4332BSE is a high-performance, 32-bit resolution, two-channel DAC. The CS4332BSE supports single-ended analog output, and 32-bit digital input via the audio serial port (ASP) at sample rates up to 384 kHz.

The voltage-output DAC incorporates a proprietary analog FIR architecture to reduce out-of-band noise and minimize the external component requirements. Low-latency digital-interpolation filters are provided. The analog output supports configurable out-of-band filtering, enabling flexible integration, and optimal dynamic range for the target application.

The CS4332BSE can be configured using a control interface supporting I²C™ and SPI™ modes of operation. The device can also be operated in hardware mode, using external resistors to select the required configuration. Multiple hardware-control options are supported, including system clocking source, ASP format, and sample rate.

The low-latency digital filters are optimized for the applicable sample rate. A de-emphasis filter is provided in the output path.

A signal-activity detection function monitors the input signal on the DAC output paths to determine signal-activity level relative to a configurable threshold. The signal-activity level status (active or idle) is reported using a dedicated pin that can be monitored by the host to enable a quick and intelligent response to the audio environment, resulting in improved system-level efficiencies and enhanced overall user experience.

The ASP supports operation in I²S, left-justified, and TDM data formats. Tristate control of the data-output pin allows multiple devices to operate on a shared bus.

Clocking for the CS4332BSE is provided by a separate clock source (MCLK) or else from the crystal oscillator. The DAC-conversion timing is referenced to the ASP data frame, enabling time-aligned operation across multiple devices sharing a common data bus.

The CS4332BSE can be powered from a single 3.3 V supply. Digital input at 1.8 V logic levels is also possible using a separate external supply. The device combines high performance with low power consumption.

The CS4332BSE is available in a commercial-grade 0.4 mm pitch, 40-pin QFN package for operation from –40 °C to +85 °C.

See Section 11 for ordering information.

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1 Pin Assignments and Descriptions

1.1 40-Pin QFN (Top View, Through-Package)

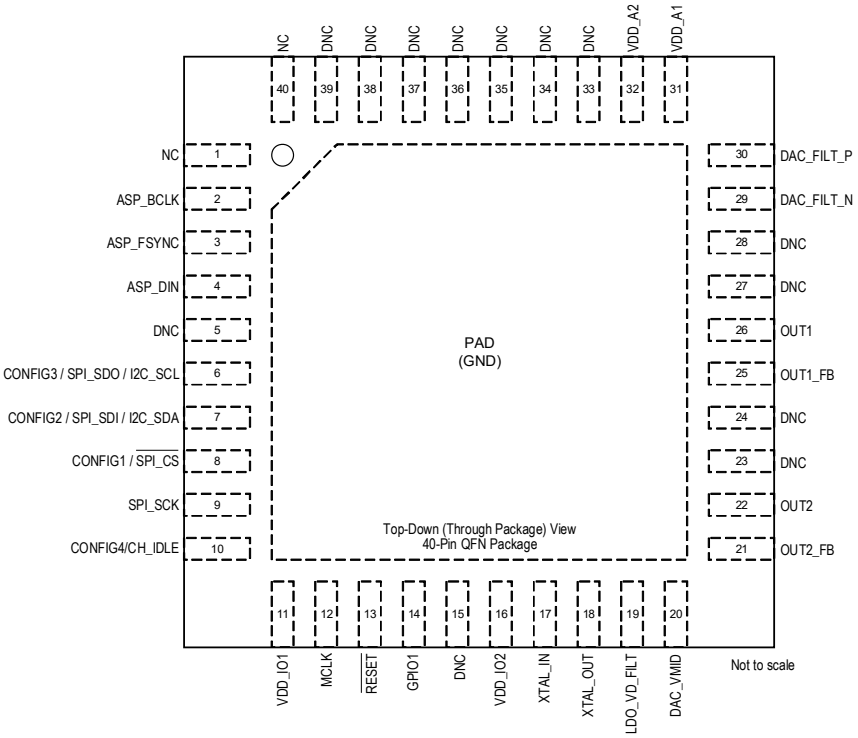

Figure 1-1. QFN 40-Pin Diagram (Top View, Through Package)

1.2 QFN Pin Descriptions

Table 1-1. QFN Pin Descriptions

Pin Name	Pin #	Power Supply	I/O	Description
				Digital I/O
ASP_BCLK	2	VDD_IO1	I/O	Audio serial port bit clock.
ASP_DIN	4	VDD_IO1	I	Audio serial port data input.
ASP_FSYNC	3	VDD_IO1	I/O	Audio serial port frame sync.
GPIO1	14	VDD_IO2	I/O	General-purpose input/output.
MCLK	12	VDD_IO1	I/O	Main clock input/output.
$\overline{\text{RESET}}$	13	VDD_IO1	I	Hardware reset control (active low).
XTAL_IN	17	VDD_IO2	I/O	Input for an external crystal/General-purpose input/output.
XTAL_OUT	18	VDD_IO2	I/O	Output for an external crystal/General-purpose input/output.
				Analog I/O
CONFIG1/$\overline{\text{SPI_CS}}$	8	VDD_IO1	I	Hardware control pins.
CONFIG2/SPI_SDI/I2C_SDA	7	VDD_IO1	I/O	In software control mode, CONFIG1 to CONFIG3 support the SPI/I^{2}C interface.
CONFIG3/SPI_SDO/I2C_SCL	6	VDD_IO1	I/O	
CONFIG4/CH_IDLE	10	VDD_IO1	I/O	In software control mode, CONFIG1 selects the I^{2}C target address.
SPI_SCK	9	VDD_IO1	I	In software control mode, CONFIG4 supports Signal Activity Detection. SPI clock input.

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Table 1-1. QFN Pin Descriptions *(Cont.)*

Pin Name	Pin #	Power Supply	I/O	Description
DAC_FILT_N DAC_FILT_P	29 30	VDD_A1 VDD_A1	O O	DAC external capacitor connection. Connect the DAC_FILT_P capacitor to VDD_A1.
DAC_VMID	20	VDD_A1	O	DAC mid-rail voltage reference output.
LDO_VD_FILT	19	VDD_A2	O	LDO_D regulator external capacitor connection.
OUT1 OUT2	26 22	VDD_A1 VDD_A1	O O	Analog output.
OUT1_FB OUT2_FB	25 21	VDD_A1 VDD_A1	O O	Analog output feedback connection.
				Power Supplies
VDD_A1	31	—	—	Analog Supply 1.
VDD_A2	32	—	—	Analog Supply 2.
VDD_IO1	11	—	—	Digital I/O Supply 1.
VDD_IO2	16	—	—	Digital I/O Supply 2.
GND	PAD	—	—	Ground [1].
				No Connect
DNC	5, 15, 23, 24, 27, 28, 33, 34, 35, 36, 37, 38, 39	—	—	Do not connect.
NC	1,40	—	—	No connection, it is recommended to connect to GND.

1. The ground paddle must be tied to a common ground plane directly underneath the CS4332BSE. The ground paddle should be connected to the ground plane using at least five vias.

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1.3 Termination of Unused Pins

Table 1-2 shows the required termination for unused pins (i.e., if the functionality of the pin is not being used). Pins not listed must be connected as shown in the typical connection drawings (see Section 2).

Table 1-2. Termination of Unused Pins

Name	Termination if unused
MCLK [1]	Float
CONFIG3/SPI_SDO/I2C_SCL	10 kΩ pull-down to GND
CONFIG4/CH_IDLE	
GPIO1	
SPI_SCK	
XTAL_IN	
XTAL_OUT	
OUTn	Connect to OUTn_FB
$\overline{\text{RESET}}$	Connect to VDD_IO1

1. If the system clock is provided by the crystal oscillator and an MCLK output is not required, MCLK should be left floating.

1.4 Electrostatic Discharge (ESD) Protection

ESD-sensitive device. The CS4332BSE is manufactured on a CMOS process. Therefore, it is generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken while handling and storing this device. This device is qualified to current JEDEC ESD protection standards.

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2 Typical Connections Diagram

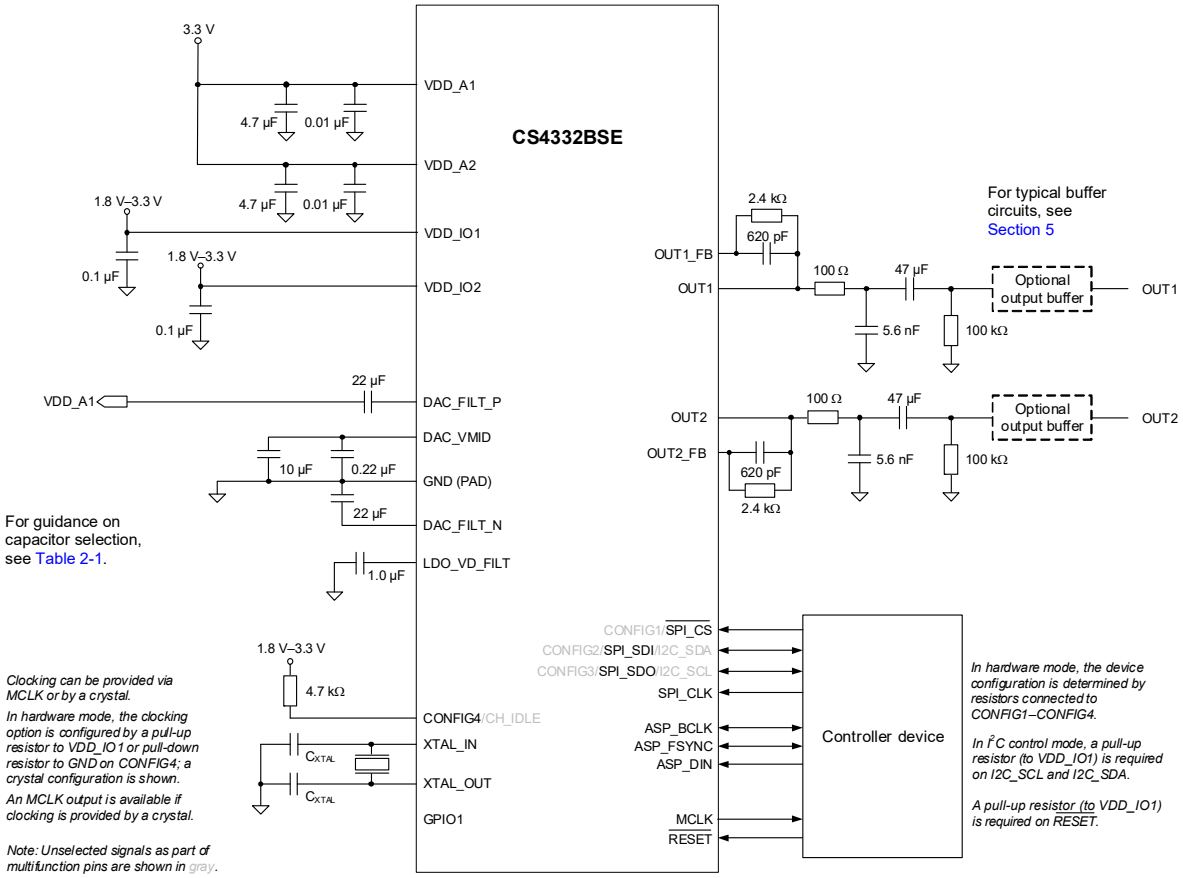

Figure 2-1. Typical Connections

Guidance on capacitor selection is provided in Table 2-1:

Table 2-1. External Component Requirements

Connection	Capacitor	Requirements
LDO_VD_FILT	1.0 µF ceramic	Must not derate below 0.8 µF at 1.2 V
DAC_FILT	22 µF ceramic	Must not derate below 6.8 µF at 3.3 V
DAC_VMID	0.22 µF ceramic	Must not derate below 0.1 µF at 1.65 V
	10 µF ceramic	Must not derate below 5 µF at 1.65 V
VDD_A	0.01 µF ceramic	—
	4.7 µF ceramic	—
VDD_IO	0.1 µF ceramic	—

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3 Characteristics and Specifications

Note: Table 3-1 defines parameters as they are characterized in this section. Default register field configurations are used unless specified otherwise in the test conditions.

Table 3-1. Parameter Definitions

Parameter	Definition
Channel separation	The difference in level between the active channel (driven to maximum full scale output) and the measured signal level in the idle channel at the test signal frequency. The active channel is configured and supplied with an appropriate input signal to drive a full scale output, with signal measured at the output of the associated idle channel.
Dynamic range	The difference in level between the maximum full-scale output signal and the sum of all harmonic distortion products plus noise with a low-level input signal applied (an input signal level 60 dB below full scale is used).
Power-supply rejection ratio (PSRR)	The ratio of a specified power supply variation relative to the output signal that results from it. PSRR is measured under quiescent signal path conditions.
Total harmonic distortion plus noise (THD+N)	The ratio of the RMS sum of the harmonic distortion products plus noise in the specified bandwidth relative to the RMS amplitude of the fundamental (i.e., test frequency) output.

Note: Unless specified otherwise, all performance measurements are for a 20 Hz to 20 kHz bandwidth.

Table 3-2. Recommended Operating Conditions

Test conditions (unless specified otherwise): Ground = GND = 0 V; voltages are with respect to ground.

Parameter		Symbol	Minimum	Maximum	Unit
DC power supply	Analog supply [1]	VDD_A1, VDD_A2	3.13	3.47	V
	Digital I/O supply	VDD_IO1, VDD_IO2	1.71	3.63	V
Supply ramp up/down (all supplies)		t_{PWR-UD}	0.01	10	ms
Ambient temperature		T_A	–40	85	°C

Note: Functionality and parametric performance is not guaranteed or implied outside of the limits in this table. Operation outside of these limits may adversely affect device reliability.

1. The VDD_A1 and VDD_A2 rails should be tied together and powered from a single supply. The associated power domain is referred to as VDD_A.

Table 3-3. Absolute Maximum Ratings

Test conditions (unless specified otherwise in this table): Ground = GND = 0 V; voltages are with respect to ground.

Parameter		Symbol	Minimum	Maximum	Unit
DC power supply	Analog supply [1]	VDD_A1, VDD_A2	–0.3	4.32	V
	Digital core	LDO_VD_FILT	–0.3	1.52	V
	Digital I/O supply	VDD_IO1, VDD_IO2	–0.3	4.32	V
External voltage applied to digital input/output	VDD_IO1 logic pins VDD_IO2 logic pins	V_{INDI}	–0.3 –0.3	VDD_IO1 + 0.3 VDD_IO2 + 0.3	V V
External voltage applied to analog inputs		V_{INAI}	–0.3	VDD_A + 0.3	V
Input current	digital input/output analog inputs	I_{IN}	— —	±10 ±10	mA mA
Ambient operating temperature		T_A	–40	+115	°C
Junction operating temperature		T_J	–40	+125	°C
Storage temperature		T_{STG}	–65	+150	°C

Caution: Stresses beyond “Absolute Maximum Ratings” levels may cause permanent damage to the device. These levels are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Table 3-2 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1. The VDD_A1 and VDD_A2 rails should be tied together and powered from a single supply. The associated power domain is referred to as VDD_A.

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Table 3-4. DAC Path Characteristics

Test conditions (unless specified otherwise in this table): External components as shown in Fig. 2-1 incorporating the typical output circuit illustrated in Fig. 5-1; VDD_A = VDD_IO1 = VDD_IO2 = 3.3 V; Ground = GND = 0 V; voltages are with respect to ground; T_A = +25 ºC; 1 kHz sine wave test signal; output load = 3 kΩ; Fs = 48 kHz, 32-bit audio data, MCLK = 24.576 MHz.

Parameter			Min	Typ	Max	Units
Full scale output signal level (OUTn)		0 dBFS input	—	1.00	—	V_{RMS}
Dynamic range		A-weighted	107	115	—	dB
		unweighted	104	112	—	dB
THD+N	Output load = 3 kΩ	0 dBFS input	—	–102	–94	dB
		–20 dBFS input	—	–87	—	dB
		–60 dBFS input	—	–47	—	dB
THD+N	Output load = 10 kΩ	0 dBFS input	—	–107	–94	dB
		–20 dBFS input	—	–87	—	dB
		–60 dBFS input	—	–47	—	dB
Idle channel noise		A-weighted	—	3.16	—	μV_{RMS}
Channel separation		1 kHz	—	110	—	dB
		20 kHz	—	100	—	dB
PSRR (VDD_A)		100 mV (peak-peak) 1 kHz sine wave	—	75	—	dB
Load resistance			3	10	—	kΩ
Load capacitance			—	—	100	pF

Table 3-5. DAC Filter Characteristics

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO1 = VDD_IO2 = 3.3 V; Ground = GND = 0 V; voltages are with respect to ground; T_A = +25 ºC; 1 kHz sine wave test signal; Fs = 48 kHz, 32-bit audio data.

Parameter			Min	Typ	Max	Units
Fs = 16 kHz	Passband	to –3 dB corner	—	—	0.49	Fs
	Passband ripple	f ≤ 0.45 Fs	–0.001	—	0.001	dB
	Stopband attenuation	f ≥ 0.55 Fs	100	—	—	dB
	Group delay [1]		—	33.6/Fs	—	s
Fs = 32 kHz	Passband	to –3 dB corner	—	—	0.49	Fs
	Passband ripple	f ≤ 0.45 Fs	–0.001	—	0.001	dB
	Stopband attenuation	f ≥ 0.55 Fs	100	—	—	dB
	Group delay [1]		—	32.5/Fs	—	s
Fs = 44.1 kHz or 48 kHz	Passband	to –3 dB corner	—	—	0.47	Fs
	Passband ripple	f ≤ 0.42 Fs	–0.004	—	0.005	dB
	Stopband attenuation	f ≥ 0.59 Fs	101	—	—	dB
	Group delay [1]		—	4.6/Fs	—	s
Fs = 88.2 kHz or 96 kHz	Passband	to –3 dB corner	—	—	0.35	Fs
	Passband ripple	f ≤ 0.23 Fs	–0.001	—	0.001	dB
	Stopband attenuation	f ≥ 0.55 Fs	101	—	—	dB
	Group delay [1]		—	5.2/Fs	—	s
Fs = 176.4 kHz or 192 kHz	Passband	to –3 dB corner	—	—	0.28	Fs
	Passband ripple	f ≤ 0.11 Fs	–0.001	—	0.001	dB
	Stopband attenuation	f ≥ 0.55 Fs	109	—	—	dB
	Group delay [1]		—	6.7/Fs	—	s
Fs = 352.8 kHz or 384 kHz	Passband	to –3 dB corner	—	—	0.22	Fs
	Passband ripple	f ≤ 0.06 Fs	–0.001	—	0.000	dB
	Stopband attenuation	f ≥ 0.55 Fs	116	—	—	dB
	Group delay [1]		—	7.6/Fs	—	s

1. Group delay is measured from the start of the FSYNC frame containing the audio data on the ASP_DIN pin to the time at which the signal is presented on the output pins (OUTn).

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Table 3-6. DAC High-Pass Filter (HPF) Characteristics

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO1 = VDD_IO2 = 3.3 V; Ground = GND = 0 V; voltages are with respect to ground; T_A = +25 ºC; 1 kHz sine wave test signal; Fs = 48 kHz, 32-bit audio data.

Parameter		Min	Typ	Max	Units
Passband	–0.01 dB corner	—	19	—	Hz
	–3 dB corner	—	1	—	Hz
Filter settling time		—	0.4	—	s

Table 3-7. Device Power Consumption

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO1 = VDD_IO2 = 3.3 V; Ground = GND = 0 V; voltages are with respect to ground; T_A = +25 ºC; 1 kHz sine wave test signal; ASP Secondary Mode; Fs = 48 kHz, 32-bit audio data.

Use Configuration		Typical Current (mA)			Total Power (mW)
		I_{VDD_A}	I_{VDD_IO1}	I_{VDD_IO2}	
Reset	$\overline{RESET}$ = Logic 0	0.24	0.08	0.001	1.06
Two DAC channels enabled		30	0.8	0.001	101.64

Table 3-8. Digital Interface Specifications and Characteristics

Test conditions (unless specified otherwise in this table): Ground = GND = 0 V; voltages are with respect to ground; T_A = +25 ºC.

Parameter		Symbol	Minimum	Maximum	Unit
Input leakage current (per pin)		I_{IN}	—	±10	µA
Input capacitance (per pin)		C_{IN}	—	5	pF
Digital I/O (VDD_IO1 logic pins; see Section 1)	High-level output	V_{OH}	0.9×VDD_IO1	—	V
	Low-level output	V_{OL}	—	0.1×VDD_IO1	V
	High-level input	V_{IH}	0.7×VDD_IO1	—	V
	Low-level input	V_{IL}	—	0.3×VDD_IO1	V
Digital I/O (VDD_IO2 logic pins; see Section 1)	High-level output	V_{OH}	0.9×VDD_IO2	—	V
	Low-level output	V_{OL}	—	0.1×VDD_IO2	V
	High-level input	V_{IH}	0.7×VDD_IO2	—	V
	Low-level input	V_{IL}	—	0.3×VDD_IO2	V

Table 3-9. DC Characteristics

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO1 = VDD_IO2 = 3.3 V; Ground = GND = 0 V; voltages are with respect to ground; T_A = +25 ºC.

Parameter			Minimum	Typical	Maximum	Unit
LDO_VD_FILT	Nominal voltage		—	1.2	—	V
DAC_FILT	Nominal voltage	VDD_A to DAC_FILT_P	—	1.95	—	V
		DAC_FILT_N to GND	—	1.9	—	V
DAC_VMID	Nominal voltage		—	1.65	—	V
	Maximum output current		—	50	—	nA
VDD_A power-on reset (POR) threshold (V_{POR})		VDD_A rising	2.0	—	2.8	V
		VDD_A falling	2.0	—	2.8	V
VDD_IO1 power-on reset (POR) threshold (V_{POR})		VDD_IO1 rising	1.08	—	1.58	V
		VDD_IO1 falling	0.99	—	1.43	V
VDD_IO2 power-on reset (POR) threshold (V_{POR})		VDD_IO2 rising	0.45	—	0.77	V
		VDD_IO2 falling	0.45	—	0.77	V

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Table 3-10. Switching Specifications—Reset and Clock References

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO1 = VDD_IO2 = 3.3 V; Ground = GND = 0 V; voltages are with respect to ground; T_A = +25 ºC.

Parameter		Symbol	Minimum	Typical	Maximum	Unit
Reset	$\overline{\text{RESET}}$ low (logic 0) pulse width	t_{RLPW}	1	—	—	ms
	$\overline{\text{RESET}}$ rising edge to control port active	t_{IRS}	—	—	5	ms
MCLK input	MCLK frequency	f_{MCLK}	— — — —	24.576 22.5792 49.152 45.1584	— — — —	MHz MHz MHz MHz
	MCLK duty cycle	D_{MCLK}	45	—	55	%
	MCLK frequency tolerance	—	–1	—	1	%
MCLK output	MCLK frequency	f_{MCLK}	— — — —	24.576 22.5792 49.152 45.1584	— — — —	MHz MHz MHz MHz
	MCLK duty cycle	D_{MCLK}	45	—	55	%
	MCLK frequency accuracy	—	–1	—	1	%
Crystal	Oscillator frequency	f_{XTAL}	— — — —	24.576 22.5792 49.152 45.1584	— — — —	MHz MHz MHz MHz
	Interface transconductance VDD_IO2 = 3.3 V VDD_IO2 = 1.8 V	—	— —	26 43	— —	mS mS

Table 3-11. Switching Specifications—Audio Serial Port (ASP)

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO2 = 3.3 V; Ground = GND = 0 V; voltages are with respect to ground; input timings are measured at V_{IL} and V_{IH} thresholds, output timings are measured at V_{OL} and V_{OH} thresholds for VDD_IO1 logic (as specified in Table 3-8); T_A = 25 °C.

Parameter [1,2]		Symbol	Minimum	Maximum	Unit
Secondary Mode, VDD_IO1 = 3.3 V	ASP_FSYNC input sample/frame rate	Fs	16	384	kHz
	ASP_FSYNC pulse width	$t_{HI:FSYNC}$	$1/f_{ASP_BCLK}$	—	ns
	ASP_BCLK frequency	f_{BCLK}	1.024	24.576	MHz
	ASP_BCLK high period	$t_{HI:BCLK}$	18	—	ns
	ASP_BCLK low period	$t_{LO:BCLK}$	18	—	ns
	ASP_FSYNC setup time before ASP_BCLK latching edge	$t_{SU:FSYNC}$	5	—	ns
	ASP_FSYNC hold time after ASP_BCLK latching edge	$t_{H:FSYNC}$	5	—	ns
	ASP_DIN setup time before ASP_BCLK latching edge	$t_{SU:DIN}$	10	—	ns
	ASP_DIN hold time after ASP_BCLK latching	$t_{H:DIN}$	5	—	ns
Primary Mode, VDD_IO1 = 3.3 V	ASP_FSYNC output sample/frame rate	Fs	16	384	kHz
	ASP_BCLK frequency	f_{BCLK}	2.8224	24.576	MHz
	ASP_BCLK duty cycle	D_{BCLK}	45	55	%
	ASP_FSYNC delay time after ASP_BCLK launching edge	$t_{D:BCLK–FSYNC}$	0	20	ns
	ASP_DIN setup time before ASP_BCLK latching edge	$t_{SU:DIN}$	6	—	ns
	ASP_DIN hold time after ASP_BCLK latching edge	$t_{H:DIN}$	5	—	ns
	ASP_DIN load capacitance ASP_BCLK ASP_FSYNC	—	0 0	50 50	pF pF
Secondary Mode, VDD_IO1 = 1.8 V	ASP_FSYNC input sample/frame rate	Fs	16	384	kHz
	ASP_FSYNC pulse width	$t_{HI:FSYNC}$	$1/f_{ASP_BCLK}$	—	ns
	ASP_BCLK frequency	f_{BCLK}	1.024	24.576	MHz
	ASP_BCLK high period	$t_{HI:BCLK}$	18	—	ns
	ASP_BCLK low period	$t_{LO:BCLK}$	18	—	ns
	ASP_FSYNC setup time before ASP_BCLK latching edge	$t_{SU:FSYNC}$	5	—	ns
	ASP_FSYNC hold time after ASP_BCLK latching edge	$t_{H:FSYNC}$	5	—	ns
	ASP_DIN setup time before ASP_BCLK latching edge	$t_{SU:DIN}$	10	—	ns
	ASP_DIN hold time after ASP_BCLK latching	$t_{H:DIN}$	5	—	ns

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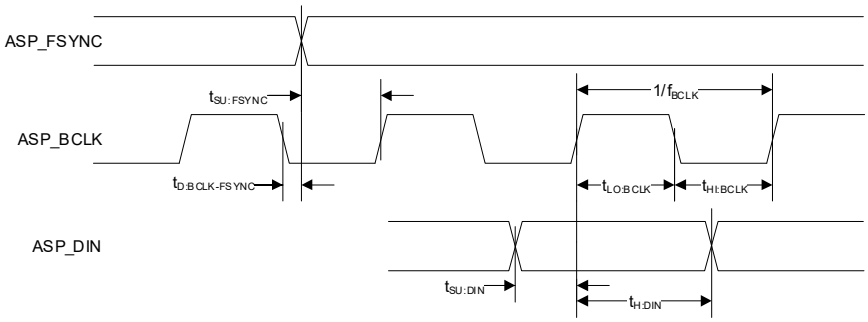
Table 3-11. Switching Specifications—Audio Serial Port (ASP) *(Cont.)*

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO2 = 3.3 V; Ground = GND = 0 V; voltages are with respect to ground; input timings are measured at V_{IL} and V_{IH} thresholds, output timings are measured at V_{OL} and V_{OH} thresholds for VDD_IO1 logic (as specified in Table 3-8); T_A = 25 °C.

Parameter [1,2]		Symbol	Minimum	Maximum	Unit
Primary Mode, VDD_IO1 = 1.8 V	ASP_FSYNC output sample/frame rate	Fs	16	384	kHz
	ASP_BCLK frequency	f_{BCLK}	2.8224	24.576	MHz
	ASP_BCLK duty cycle	D_{BCLK}	45	55	%
	ASP_FSYNC delay time after ASP_BCLK launching edge	$t_{D:BCLK–FSYNC}$	0	20	ns
	ASP_DIN setup time before ASP_BCLK latching edge	$t_{SU:DIN}$	6	—	ns
	ASP_DIN hold time after ASP_BCLK latching edge	$t_{H:DIN}$	5	—	ns
	ASP_DIN load capacitance ASP_BCLK ASP_FSYNC	—	0 0	50 50	pF pF

1. ASP timing in I²S and Left-Justified Modes.
   ASP_BCLK can be inverted if required; the figure shows the default polarity.



2. ASP timing in TDM Mode.
   ASP_BCLK can be inverted if required; the figure shows the default polarity.

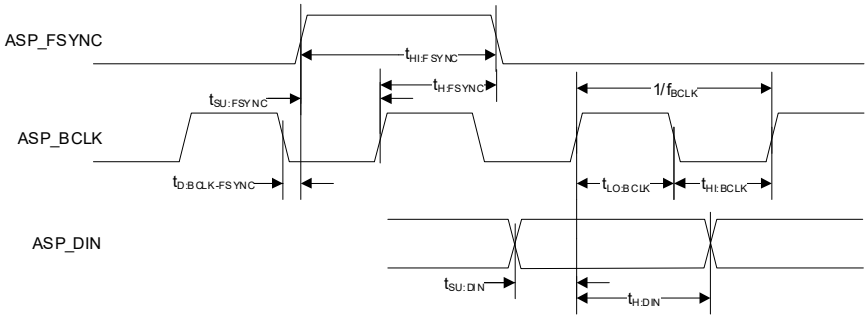


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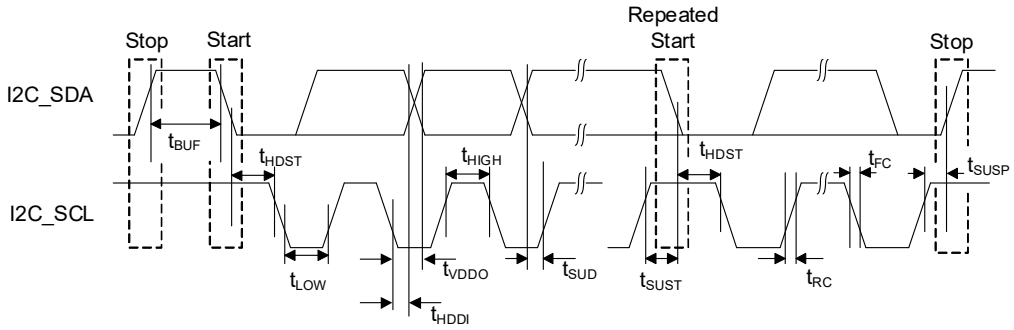
Table 3-12. Switching Specifications—I²C Control Port

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO1 = VDD_IO2 = 3.3 V; Ground = GND = 0 V; voltages are with respect to ground; input timings are measured at V_{IL} and V_{IH} thresholds, output timings are measured at V_{OL} and V_{OH} thresholds for VDD_IO1 logic (as specified in Table 3-8); T_A = 25 °C.

Parameter [1,2]		Symbol	Minimum	Maximum	Unit
SCL clock frequency		f_{SCL}	—	1000	kHz
Clock low time		t_{LOW}	500	—	ns
Clock high time		t_{HIGH}	260	—	ns
Start condition hold time (before first clock pulse)		t_{HDST}	260	—	ns
Setup time for repeated start		t_{SUST}	260	—	ns
Rise time of SCL and SDA	$f_{SCL} \le 100$ kHz 100 kHz < $f_{SCL} \le 400$ kHz 400 kHz < $f_{SCL} \le 1000$ kHz	t_{RC}	600 180 72	1000 300 120	ns ns ns
Fall time of SCL and SDA	$f_{SCL} \le 100$ kHz 100 kHz < $f_{SCL} \le 400$ kHz 400 kHz < $f_{SCL} \le 1000$ kHz	t_{FC}	6.5 6.5 6.5	300 300 120	ns ns ns
Rise time variation between SDA and SCL		—	—	1.67	ns
Fall time variation between SDA and SCL	$f_{SCL} \le 100$ kHz 100 kHz < $f_{SCL} \le 400$ kHz 400 kHz < $f_{SCL} \le 1000$ kHz	—	— — —	100 100 75	ns ns ns
Setup time for stop condition		t_{SUSP}	260	—	ns
SDA setup time to SCL rising		t_{SUD}	50	—	ns
SDA input hold time from SCL falling [3]		t_{HDDI}	0	—	ns
Output data valid (Data/ACK) [4]	$f_{SCL} \le 100$ kHz 100 kHz < $f_{SCL} \le 400$ kHz 400 kHz < $f_{SCL} \le 1000$ kHz	t_{VDDO}	— — —	3450 900 450	ns ns ns
Bus free time between transmissions		t_{BUF}	500	—	ns
SDA bus capacitance		C_B	—	550	pF
SCL/SDA pull-up resistance		R_P	500	—	Ω
Pulse width of spikes to be suppressed		t_{ps}	0	50	ns

1. All timing is relative to thresholds specified in Table 3-8, V_{IL} and V_{IH} for input signals, and V_{OL} and V_{OH} for output signals.
2. I²C control-port timing.



3. Data must be held long enough to bridge the transition time, t_{FC}, of SCL.
4. Time from falling edge of SCL until data output is valid.

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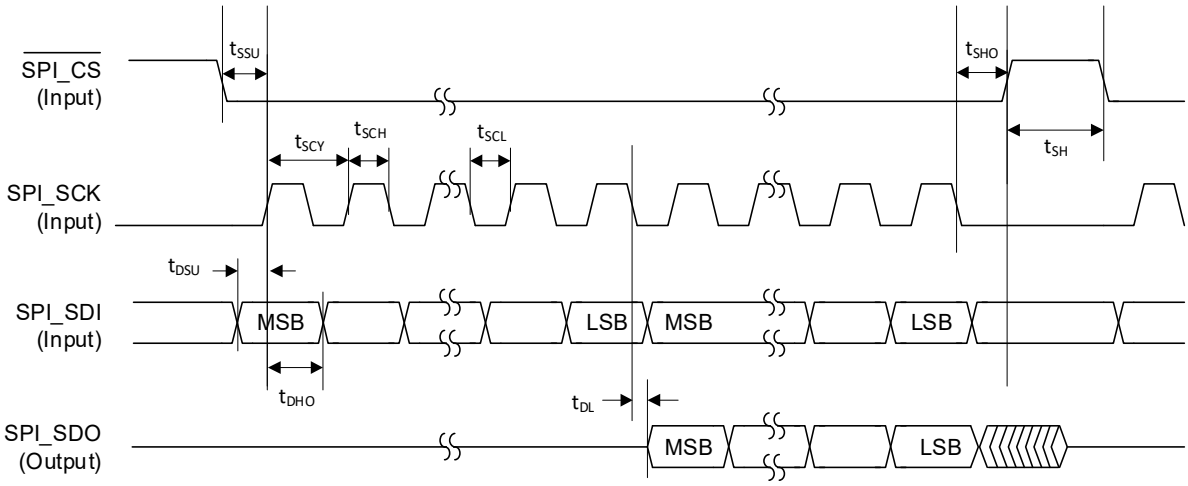
Table 3-13. Switching Specifications—SPI Control Port

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO1 = VDD_IO2 = 3.3 V; Ground = GND = 0 V; voltages are with respect to ground; input timings are measured at V_{IL} and V_{IH} thresholds, output timings are measured at V_{OL} and V_{OH} thresholds for VDD_IO1 logic (as specified in Table 3-8); T_A = 25 °C.

Parameter [1]	Symbol	Minimum	Maximum	Unit
SPI_SCK frequency	f_{SCY}	—	24	MHz
$\overline{\text{SPI_CS}}$ falling edge to SPI_SCK rising edge	t_{SSU}	5	—	ns
SPI_SCK falling edge to $\overline{\text{SPI_CS}}$ rising edge	t_{SHO}	0.5	—	ns
SPI_SCK pulse width low	t_{SCL}	18.5	—	ns
SPI_SCK pulse width high	t_{SCH}	18.5	—	ns
SPI_SDI to SPI_SCK setup time	t_{DSU}	5	—	ns
SPI_SDI to SPI_SCK hold time	t_{DHO}	2.5	—	ns
SPI_SCK falling edge to SPI_SDO transition	t_{DL}	0	15	ns
$\overline{\text{SPI_CS}}$ rising edge to SPI_SDO output high-Z	—	0	15	ns
Bus free time between active $\overline{\text{SPI_CS}}$	t_{SH}	20	—	ns

1.SPI control-port timing.



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4 Functional Description

4.1 Device Power and Reset

The CS4332BSE is powered using VDD_A1, VDD_A2, VDD_IO1, and VDD_IO2 external supplies.

Notes: The VDD_A1 and VDD_A2 rails should be star-connected and powered from a single supply. The associated power domain is referred to as VDD_A.

VDD_IO1 and VDD_IO2 are independent power domains. VDD_IO1 supplies host-related interfaces (e.g., SPI control interface); VDD_IO2 supplies external interfaces (e.g., crystal oscillator connections). Integrated level shifters are included for direct interface to logic levels from 1.8 V to 3.3 V.

There are no power-sequencing requirements—supplies can be enabled in any order.

The CS4332BSE is in reset if the $\overline{\text{RESET}}$ pin is asserted (Logic 0), or if the VDD_A supply is below the respective reset threshold defined in Table 3-9.

The ground paddle, must be tied to a common ground (GND) plane directly underneath the CS4332BSE.

4.2 Hardware Configuration

The CS4332BSE supports hardware and software control modes. In hardware mode, the device configuration is determined entirely by external resistors connected to the hardware-control pins. In software mode, the I²C/SPI control port is used to configure the device.

In hardware mode, the audio serial port (ASP) configuration is selected using the CONFIG1 and CONFIG2 pins as described in Table 4-1. See Section 4.4 for more details of the sample-rate selection and Section 4.7 for more details of the ASP operation.

Table 4-1. Hardware Control—ASP Configuration

Pin Name	Pin Configuration		Description
CONFIG1	Pull-up to VDD_IO1	0 Ω	Software control mode (I²C/SPI)
		4.7 kΩ	In I²C Mode, the pull-up resistor is used to select the device address—see Section 4.8.
		22 kΩ	In SPI Mode, it is recommended to use a 100 kΩ pull-up resistor.
		100 kΩ	
	Pull-down to GND	100 kΩ	ASP Primary Mode, 176.4 kHz, 192 kHz sample rate
		22 kΩ	ASP Primary Mode, 88.2 kHz, 96 kHz sample rate
		4.7 kΩ	ASP Primary Mode, 44.1 kHz, 48 kHz sample rate
		0 Ω	ASP Secondary Mode, autodetect sample rate
CONFIG2	Pull-up to VDD_IO1	0 Ω	ASP TDM Mode—minimum time slots [1], ASP_FSYNC_TYPE = pulse
		4.7 kΩ	ASP TDM Mode—maximum time slots [2], ASP_FSYNC_TYPE = pulse
		22 kΩ	—
		100 kΩ	ASP TDM Mode—minimum time slots [1], ASP_FSYNC_TYPE = square wave (50% duty cycle) [3]
	Pull-down to GND	100 k	ASP TDM Mode—maximum time slots [2], ASP_FSYNC_TYPE = square wave (50% duty cycle) [3]
		22 kΩ	—
		4.7 kΩ	ASP Left-Justified Mode
		0 Ω	ASP I²S Mode

1. The ASP data format is configured to support two time slots; this is the minimum necessary for the CS4332BSE input.
2. The ASP data format is configured to support the maximum number of time slots for the applicable BCLK rate, refer to Table 4-9.
3. ASP_FSYNC_TYPE = square wave (50% duty cycle) is available in ASP Primary Mode only, as described in Section 4.7.

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If the ASP is configured for TDM data format with maximum time slots, the TDM slot selection is determined using the CONFIG3 pin as described in Table 4-2. See Section 4.7 for more details of the ASP TDM modes.

Table 4-2. Hardware Control—TDM Slot Selection

Pin Name	Pin Configuration		Description
CONFIG3	Pull-up to VDD_IO1	0 Ω	Slots 14–15 [1]
		4.7 kΩ	Slots 12–13 [1]
		22 kΩ	Slots 10–11 [1]
		100 kΩ	Slots 8–9 [1]
	Pull-down to GND	100 kΩ	Slots 6–7 [2]
		22 kΩ	Slots 4–5 [2]
		4.7 kΩ	Slots 2–3
		0 Ω	Slots 0–1

1.Slots 8–15 are only valid in 16-slot TDM Mode.
2.Slots 4–7 are only valid in 8-slot or 16-slot TDM Mode.

The clock-reference configuration is determined using the CONFIG4 pin as described in Table 4-3. See Section 4.4 for more details of the CS4332BSE clocking architecture

Table 4-3. Hardware Control—Clocking Configuration

Pin Name	Pin Configuration		Clock Reference	Reference Clock Frequency (MHz)[1]
CONFIG4	Pull-up to VDD_IO1	0 Ω	XTAL	49.152 or 45.1584
		4.7 kΩ	XTAL	24.576 or 22.5792
		22 kΩ	MCLK	49.152 or 45.1584
		100 kΩ	MCLK	24.576 or 22.5792

1.The reference clock frequency is related to sample rate options (for supported configurations, see Section 4.4).

In hardware mode, the device configuration is latched when reset is released (either power-on reset or deassertion of the $\overline{\text{RESET}}$ pin). In hardware mode, the configuration cannot be changed while the device is operational. To update the device configuration, the $\overline{\text{RESET}}$ pin must be asserted (Logic 0), or the device power cycled, in order to read new settings on the CONFIGx pins.

If software mode is selected (i.e., CONFIG1 is pulled-up to VDD_IO1), the device configuration is controlled by register writes via the applicable control interface, as described in Section 4.8. Unused CONFIGx pins should be terminated as described in Section 1.3.

Note: In software mode, the CONFIG1 pin is used to select the I²C target address (see Section 4.8). If the SPI control interface is used, it is recommended to connect the CONFIG1 pin to VDD_IO1 via a 100 kΩ resistor.

4.3 Software Configuration

Software control mode is enabled if the CONFIG1 pin is pulled-up to VDD_IO1; note that $\overline{\text{RESET}}$ must remain asserted (i.e., Logic 0) until CONFIG_1/$\overline{\text{SPI_CS}}$ is deasserted (i.e., Logic 1). In software control mode, the CS4332BSE is configured by writing to control registers using the control port.

The control port supports I²C and SPI modes of operation; the applicable mode is detected automatically on the respective interface pins. In I²C mode, the target address is selectable using the CONFIG1 pin. See Section 4.8 for further details of the I²C/SPI control port.

In software control mode, GLOBAL_EN is used as the global control field for enabling/disabling the CS4332BSE functions. The device should be configured using the applicable control registers before setting GLOBAL_EN.

Notes: The clocking (Section 4.4) and ASP (Section 4.7) control registers are only valid on the rising edge of GLOBAL_EN. Writing to these registers has no effect at any other time. It is recommended to select the disabled state (GLOBAL_EN = 0) before writing to these registers.

To minimize the CS4332BSE power consumption when all output paths are disabled, see Section 4.5.4.

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A reset of the CS4332BSE can be triggered by writing 0x5A to the SW_RESET field. A software reset disables all functions and sets the control registers to their default states.

4.4 System Clocking

Clocking for the CS4332BSE is provided using either the MCLK input or the crystal (XTAL) oscillator. In each case, the frequency is related to sample rate options, as described in Table 4-4:

Table 4-4. Reference Frequency and Sample Rate Options

Reference Source	Reference Frequency (MHz)	Sample Rate (kHz)[1]
MCLK or XTAL	22.5792 or 45.1584	44.1, 88.2, 176.4, 352.8
	24.576 or 49.152	16, 32, 48, 96, 192, 384

1. Sample rates 352.8 kHz and 384 kHz are supported in software control mode only (for details of software control mode, see Section 4.4.2).

The specifications for the clocking sources are described in Table 3-10; for optimal out-of-band noise performance a reference frequency of 49.152 MHz or 45.1584 MHz is recommended.

In hardware mode, the clock source is configured using the CONFIG4 pin, as detailed in Table 4-3. In software mode, the clocking source is selected using SYSCLK_SRC.

The crystal oscillator uses an external crystal to generate the system clock. Load capacitors are connected to the crystal as shown in Fig. 4-1. A series resistor (R_S) may also be required to configure the drive level for the selected crystal.

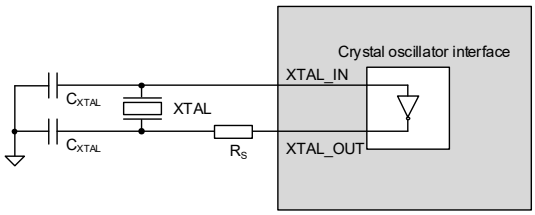

Figure 4-1. Crystal Oscillator Connection

Guidance on selecting a suitable crystal and associated components is provided in Section 5.3.1. The suitability of the external crystal is calculated as a function of the operating voltage (VDD_IO2) and the transconductance of the crystal interface, as defined in Table 3-10.

If clocking is provided using the crystal oscillator, the CS4332BSE outputs a clock on the MCLK pin. The frequency of the MCLK output clock matches the crystal oscillator frequency. The output clock can be used to drive other devices.

In ASP Secondary Mode, the ASP_FSYNC input is used to control the DAC-conversion timing, enabling multiple CS4332BSE devices to operate synchronously (sample timing is phase aligned) in a system. The external clocks ASP_FSYNC and ASP_BCLK must be derived from a common clock source (i.e., the MCLK input, or the MCLK output when clocking is provided using the crystal oscillator). See Section 4.7 for more details of the ASP.

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The clocking architecture is illustrated in Fig. 4-2.

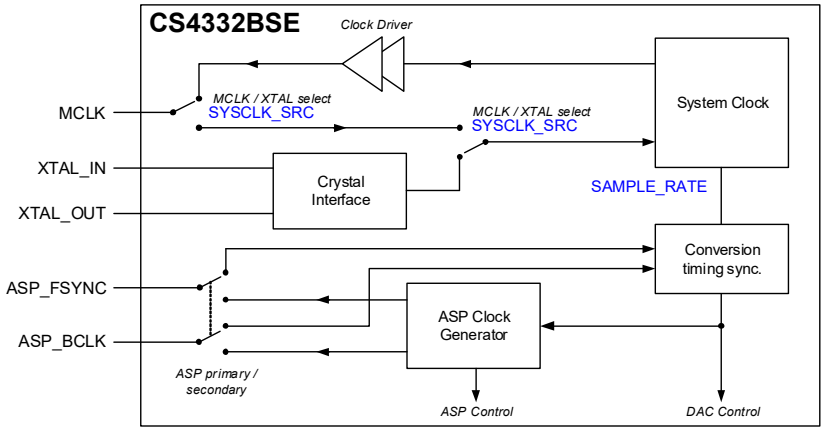

Figure 4-2. System Clocking

4.4.1 Hardware Control Mode

In hardware control mode, the system clock can be sourced from the MCLK pin or from the crystal oscillator. In each case, the frequency must be:

- 49.152 MHz or 24.576 MHz for sample rates of 16, 32, 48, 96, or 192 kHz
- 45.1584 MHz or 22.5792 MHz for sample rates of 44.1, 88.2, or 176.4 kHz

The clock source is configured using the CONFIG4 pin as described in Section 4.2.

The sample rate is selected using the CONFIG1 pin as described in Section 4.2. Sample rates 44.1 kHz–192 kHz can be configured, or else the autodetect option (sample rates 16 kHz–192 kHz) automatically configures the device according to the ASP interface clock signals. The autodetect sample-rate option is only valid if the ASP is operating in Secondary Mode (see Section 4.7).

The supported clocking configurations are summarized in Table 4-5.

Table 4-5. System Clock Configuration

Reference Source	Reference Frequency (MHz)	ASP Operating Conditions [1]
MCLK or XTAL	24.576 or 49.152	Primary or Secondary Mode, I²S, left-justified, or TDM data formats, sample rates 48, 96, and 192 kHz Primary Mode, or sample rates 16, 32, 48, 96, and 192 kHz in Secondary Mode (autodetect only).
MCLK or XTAL	22.5792 or 45.1584	Primary or Secondary Mode, I²S, left-justified, or TDM data formats, sample rates 44.1, 88.2, and 176.4 kHz in Primary Mode, or sample rates 44.1, 88.2, 176.4 kHz in Secondary Mode (autodetect only).

1. See Section 4.7 for details of the audio serial port (ASP).

The sample rate must be related to the system clock reference as described in Table 4-6.

Table 4-6. Hardware Control Mode Sample Rate Options

Reference Source	Reference Frequency (MHz)	MCLK Out (MHz)	Sample Rate (kHz)
MCLK	22.5792 or 45.1584	—	44.1, 88.2, 176.4
	24.576 or 49.152		16, 32, 48, 96, 192
XTAL	22.5792 or 45.1584	22.5792 or 45.1584	44.1, 88.2, 176.4
	24.576 or 49.152	24.576 or 49.152	16, 32, 48, 96, 192

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If the ASP is configured in ASP Secondary Mode, the external clocks (MCLK, BCLK, and FSYNC) must be derived from a common clock source and the active BCLK edge must be aligned with the falling MCLK edge. If clocking for the CS4332BSE is provided using the crystal oscillator, then the BCLK and FSYNC signals should be derived from the common clock source provided by the CS4332BSE MCLK output, see Section 4.7.

4.4.2 Software Control Mode

In software (I²C/SPI) control mode, the clocking configuration is selected using the following control fields:

- The sample rate is configured using SAMPLE_RATE. Sample rates 16 kHz–384 kHz can be configured, or else the autodetect option automatically configures the device according to the ASP interface signals. The sample-rate autodetect option is only valid for sample rates 16 kHz–192 kHz.
- The system clock source is selected using SYSCLK_SRC. The clock source can be either the crystal oscillator or MCLK.
- The system clock frequency is configured using SYSCLK_FREQ. The system clock frequency must be
  - 49.152 MHz or 24.576 MHz for sample rates of 16, 32, 48, 96, 192, or 384 kHz
  - 45.1584 MHz or 22.5792 MHz for sample rates of 44.1, 88.2, 176.4, or 352.8 kHz.

The sample rate must be related to the system clock reference as described in Table 4-7.

Table 4-7. Software Control Mode Sample Rate Options

Reference Source	Reference Frequency (MHz)	MCLK Out (MHz)	Sample Rate (kHz)
MCLK	22.5792 or 45.1584	—	44.1, 88.2, 176.4, 352.8
	24.576 or 49.152		16, 32, 48, 96, 192, 384
XTAL	22.5792 or 45.1584	22.5792 or 45.1584	44.1, 88.2, 176.4, 352.8
	24.576 or 49.152	24.576 or 49.152	16, 32, 48, 96, 192, 384

The sample-rate autodetect option (16 kHz–192 kHz) is only valid if the ASP is operating in Secondary Mode (see Section 4.7).

If the ASP is configured in ASP Secondary Mode, the external clocks (MCLK, BCLK, and FSYNC) must be derived from a common clock source and the active BCLK edge must be aligned with the falling MCLK edge. If clocking for the CS4332BSE is provided using the crystal oscillator, then the BCLK and FSYNC signals should be derived from the common clock source provided by the CS4332BSE MCLK output, see Section 4.7.

4.5 DAC and Analog Output

The CS4332BSE supports up to two analog output channels, each incorporating a high-performance sigma-delta digital-to-analog converter (DAC). Digital volume and mute control is provided on each output channel.

The digital volume and mute controls are supported in software (I²C/SPI) control mode only. In hardware control mode, all channels are enabled with 0 dB volume.

4.5.1 Path Enable

The analog outputs and DAC paths are enabled using OUTx_DAC_EN (where x indicates the channel number 1–2).

When the output paths are enabled for the first time after power-up or after the DAC reference has been disabled (described in Section 4.5.4), the paths do not become active until a startup delay has elapsed; the delay ensures the noise floor of the output path has settled before it becomes active and mitigates any audible artifacts. The time delay (1 s) is applied when the output paths are enabled using OUTx_DAC_EN.

The polarity of the DAC output can be inverted using OUTx_INV for the respective channel.

The CS4332BSE supports a mono output configuration; this can be used in applications where stereo sound is unnecessary, such as voice playback, alarms, or devices with a single speaker. If mono operation is required, it is recommended to configure the CS4332BSE with a single output path enabled prior to initial startup to minimize any audible artifacts.

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4.5.2 Digital Volume and Mute

The signal path incorporates a digital volume control, supporting a range of –127.5 dB to 0 dB in 0.5 dB steps. Volume ramping and digital mute is also supported.

The digital volume is configured using OUTx_VOL for the respective output channel. The digital mute is enabled by setting OUTx_MUTE.

Writing to the volume or mute fields has no effect on the signal path until a 1 is written to OUT_VU. Writing 1 to OUT_VU causes the volume and mute settings to be updated on all output paths simultaneously.

When the volume or mute is changed, the gain of the affected signal paths is ramped up or down to the new setting. For increasing gain, the rate is controlled by OUT_RAMP_RATE_INC; for decreasing gain, the rate is controlled by OUT_RAMP_RATE_DEC.

Note: The OUT_RAMP_RATE_INC and OUT_RAMP_RATE_DEC fields should not be changed while a volume ramp is in progress.

4.5.3 Power Optimization

A Class A amplifier is provided in the output path to convert the current output to a voltage output. An external feedback circuit is required, as described in Section 5.1.

A voltage output of 1 V_{RMS} is provided; this supports a minimum resistive load of 3 kΩ in parallel with a maximum capacitive load of 100 pF. If the load has a higher impedance, the CS4332BSE can optimize power consumption by adjusting the drive current while maintaining an output of 1 V_{RMS}. In this case, a minimum resistive load of 10 kΩ in parallel with a maximum capacitive load of 100 pF is supported.

The maximum load impedance is selected using OUT_LOAD_CFG.

4.5.4 DAC Shutdown

To minimize power consumption when all output paths are disabled, the DAC reference circuit can be disabled. Note that power consumption is only reduced if the output paths have previously been enabled. Until they are enabled for the first time, the power consumption is already minimized.

In software mode, the DAC reference circuit is disabled using DAC_SHUTDOWN. If this bit is set, all paths are disabled regardless of the status of the OUTx_DAC_EN bits. Prior to disabling the DAC reference circuit, it is recommended to mute the output paths, as described in Section 4.5.2.

Note: If the DAC_SHUTDOWN bit is cleared, any output paths where OUTx_DAC_EN is set are enabled.

In hardware mode, the DAC shutdown function incorporates a controlled shutdown sequence to mitigate any audible artifacts. The shutdown sequence slowly ramps down the digital volume and then ramps down the DAC output voltage prior to disabling the DAC reference circuit.

The shutdown sequence is selected using a rising-edge logic input on the GPIO1 pin. GPIO1 must be held low (i.e., Logic 0) during device startup.

To enable the DAC reference circuit after a hardware shutdown the $\overline{\text{RESET}}$ pin must be asserted (Logic 0), or the device power cycled.

4.6 Signal-Activity Detection

The CS4332BSE incorporates a signal-activity detection function on the DAC output paths. Signal-activity detection controls the logic level condition of the CH_IDLE output pin—the Logic 0 condition indicates signal activity on one or more input; the Logic 1 condition indicates no signal activity on all inputs.

The CH_IDLE pin is an open-drain output, allowing multiple devices to drive the Logic 0 condition in a wired-OR configuration. In a typical application, the host monitors the CH_IDLE logic level condition to determine the input signal-activity status. An external pull-up resistor, typically 10 kΩ, is required on the CH_IDLE pin.

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Signal activity is detected on the ASP input data stream of enabled DAC output paths; controls such as volume and mute have no effect on signal-activity detection. If any output paths are disabled using OUTx_DAC_EN or DAC_SHUTDOWN, signal activity on the disabled path(s) does not contribute to the logic-level condition of the CH_IDLE output pin.

Signal-activity detection is enabled on the DAC output paths by writing 0x3 to OUT_SIG_ACT_EN.

If signal-activity detection is enabled on the DAC output paths, the input signal level for each DAC output channel is monitored against a configurable signal-activity threshold. The threshold is configured for each channel using the respective OUTx_SIG_ACT_THR bits (where x indicates the channel number 1–2). If signal-activity detection is enabled on the DAC output paths, the CH_IDLE behavior is:

- If the input signal level for any output path exceeds the signal-activity threshold, CH_IDLE is driven low (Logic 0).
- If the input signal level for all output paths falls below the signal-activity threshold, CH_IDLE is pulled high (Logic 1).

Signal-activity detection uses an averaged signal level that is calculated using an exponential moving average (EMA) function. The EMA function for each DAC output channel is enabled automatically when signal-activity detection is enabled.The time constant is selected using OUT_EMA_TIME.

4.7 Audio Serial Port (ASP)

The multichannel ASP supports the input of digital audio samples to the CS4332BSE. The ASP can be configured as a primary or secondary interface, and supports I²S, left-justified, and TDM data formats.

In hardware control mode, the ASP data format is determined by the CONFIG1 and CONFIG2 pins (see Section 4.2). In software (I²C/SPI) control mode, the ASP data format is configured using register fields.

In hardware mode, sample rates 16 kHz–192 kHz are supported (sample rates 16 kHz and 32 kHz are supported using autodetect in ASP Secondary Mode only). In software mode, sample rates 16 kHz–384 kHz are supported; sample rate 384 kHz is not supported by autodetect. The supported sample rates in ASP Primary Mode and ASP Secondary Mode are summarized in Table 4-8.

Table 4-8. Supported Sample Rates in ASP Primary Mode and ASP Secondary Mode

	ASP Primary Mode		ASP Secondary Mode	
Sample Rate (kHz)	**Hardware Control Mode**	**Software Control Mode**	**Hardware Control Mode**	**Software Control Mode**
16–32	—	Configurable using SAMPLE_RATE	Determined using autodetect only	Configurable using SAMPLE_RATE (autodetect available)
44.1–192	Determined by CONFIG1 pin			
352.8, 384	—		—	Configurable using SAMPLE_RATE (autodetect not available)

4.7.1 Primary and Secondary Operation

The ASP interface can operate as a primary or secondary interface. In the primary configuration, the BCLK and FSYNC signals are generated by the CS4332BSE. In the secondary configuration, the BCLK and FSYNC pins are inputs, allowing another device to drive the respective signals.

In ASP Secondary Mode, the external clocks (MCLK, BCLK, and FSYNC) must be derived from a common clock source and the active BCLK edge must be aligned with the falling MCLK edge.

If clocking is provided by the crystal oscillator and the CS4332BSE is operating in ASP Secondary Mode, then the FSYNC and the BCLK signals should be derived from the common clock source provided by the CS4332BSE MCLK output.

In hardware control mode, the ASP is configured as a primary or secondary interface using the CONFIG1 pin (see Section 4.2). In software control mode, the ASP primary/secondary configuration is selected using ASP_PRIMARY.

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The ASP operation as a primary or secondary interface with MCLK as the clocking source is illustrated in Fig. 4-3 and Fig. 4-4.

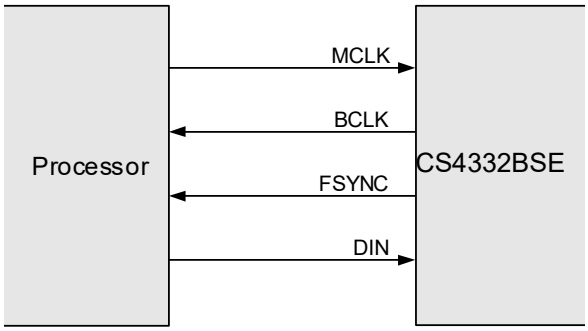

Figure 4-3. Primary Mode, MCLK Clocking Source

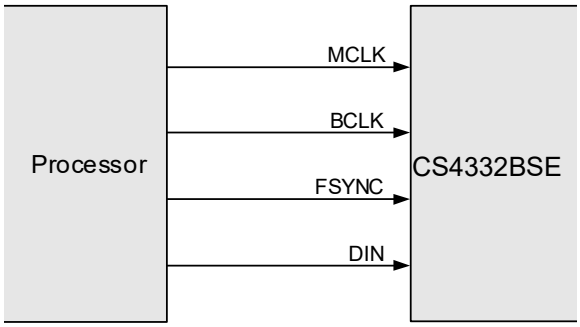

Figure 4-4. Secondary Mode, MCLK Clocking Source

The ASP operation as a primary or secondary interface with a crystal as the clocking source is illustrated in Fig. 4-5 and Fig. 4-6.

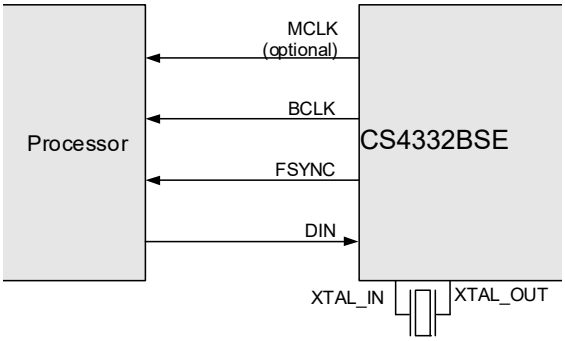

Figure 4-5. Primary Mode, XTAL Clocking Source

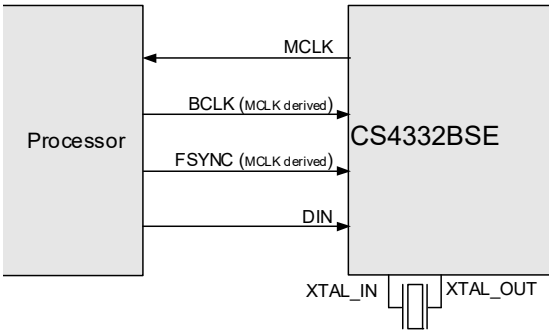

Figure 4-6. Secondary Mode, XTAL Clocking Source

4.7.2 ASP Data Formats

The ASP interface can be configured to operate in I²S, left-justified, or TDM data formats as illustrated in Fig. 4-7 through Fig. 4-9. The data-bit order is MSB first in each case; data words are encoded in 2's complement (signed, fixed-point) format. Each audio sample is allocated a time slot within the FSYNC frame.

- In I²S Mode, the MSB is valid on the second BCLK rising edge following an FSYNC transition. The other bits up to the LSB are valid on each successive BCLK cycle. Depending on word length, BCLK frequency, and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

  I²S Mode data format is shown in Fig. 4-7.

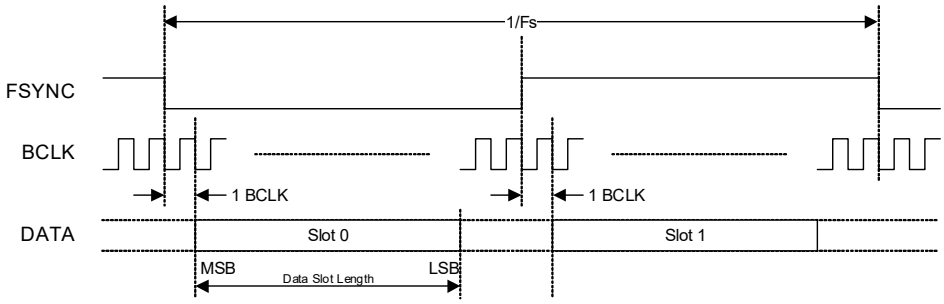

Figure 4-7. I²S Data Format

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- In Left-Justified Mode, the MSB is valid on the first BCLK rising edge following an FSYNC transition. The other bits up to the LSB are valid on each successive BCLK cycle. Depending on word length, BCLK frequency, and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

  Left-Justified Mode data format is shown in Fig. 4-8.

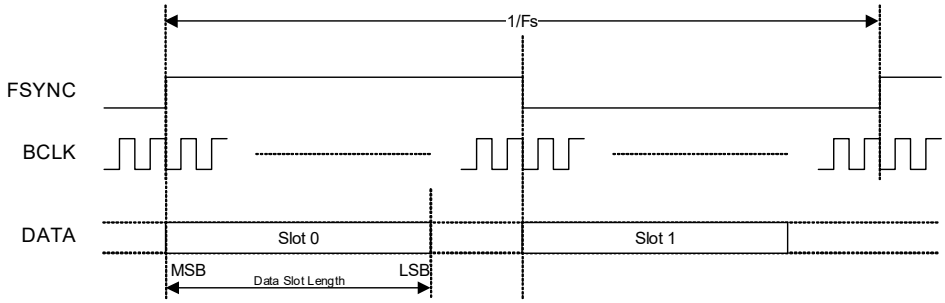

Figure 4-8. Left-Justified Data Format

- In TDM Mode, if the ASP is configured in Secondary Mode, the MSB of the first channel is valid on the second BCLK rising edge following a rising FSYNC edge. The other bits up to the LSB are valid on each successive BCLK cycle.

  If the ASP is configured in Primary Mode, the FSYNC signal can be configured as a pulse (default) or a square wave (with a 50% duty cycle). If the FSYNC signal is configured as a pulse, the MSB of the first channel is valid on the second BCLK rising edge following a rising FSYNC edge. The other bits up to the LSB are valid on each successive BCLK cycle.

  In ASP Secondary Mode and in ASP Primary Mode with the FSYNC signal configured as a pulse, the subsequent channels follow immediately after the first channel. The pulse duration can be anything less than 1/Fs, provided the falling edge of the frame pulse occurs at least one BCLK period before the rising edge of the next frame pulse. Depending on word length, BCLK frequency, and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

  TDM Mode data format in ASP Secondary Mode and ASP Primary Mode with FSYNC configured as a pulse is shown in Fig. 4-9.

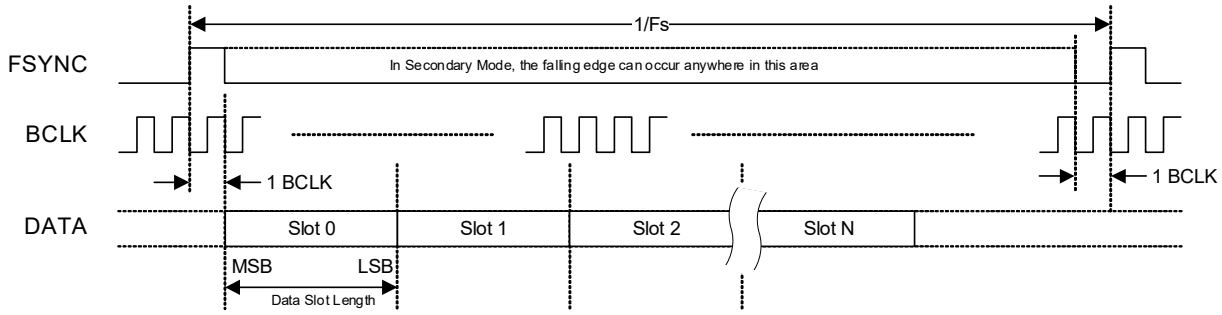

Figure 4-9. TDM Data Format Primary Mode (FSYNC = Pulse) and Secondary Mode

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In ASP Primary Mode with the FSYNC signal configured as a square wave, the slots are aligned with both rising and falling edges of FSYNC and half of the available slots occur within each phase of the FSYNC cycle. The total number of available slots is determined by the sample rate, as described in Table 4-9.

- The MSB of the first channel in each phase of the FSYNC cycle is valid on the second BCLK rising edge following the rising and falling FSYNC edge respectively. The other bits up to the LSB are valid on each successive BCLK cycle. Depending on word length, BCLK frequency, sample rate, and number of available slots, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

  TDM Mode data format in ASP Primary Mode with FSYNC configured as a square wave is shown in Fig. 4-10.

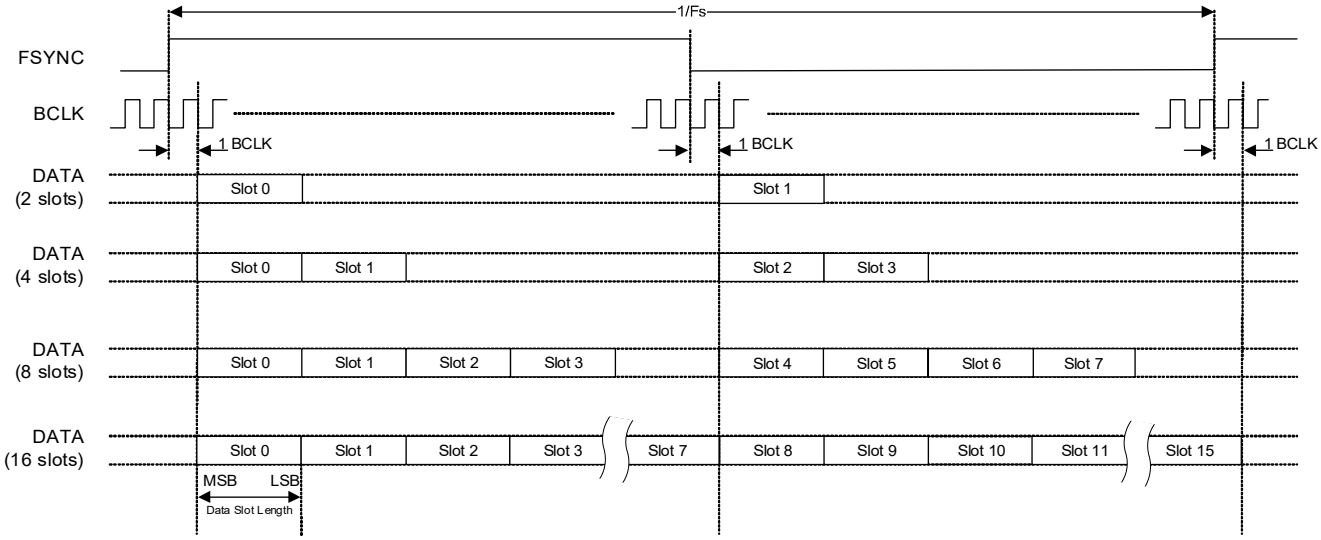

Figure 4-10. TDM Data Format Primary Mode (FSYNC = Square Wave)

4.7.3 ASP Configuration

In hardware control mode, the ASP data format is determined by the CONFIG1 and CONFIG2 pins (see Section 4.2).

In software control mode, the ASP data format is configured using SAMPLE_RATE, and ASP_FORMAT. If ASP Primary Mode is selected (see Section 4.7.1), the BCLK frequency is configured using ASP_BCLK_FREQ and the FSYNC waveform type (pulse or square wave) is configured using ASP_FSYNC_TYPE.

In software control mode, the BCLK polarity is selected using ASP_BCLK_INV. The polarity selection is valid in Primary and Secondary Modes, and determines whether the data is valid for sampling on the rising edge or the falling edge.

The BCLK polarity is illustrated in Fig. 4-11 and Fig. 4-12. In hardware control mode, the BCLK polarity is assumed to be noninverted.

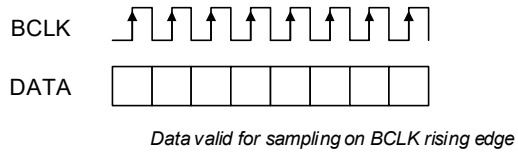

Figure 4-11. Noninverted BCLK

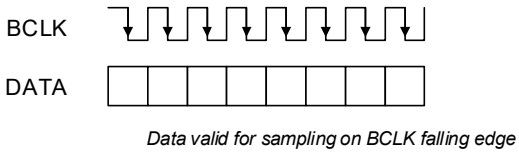

Figure 4-12. Inverted BCLK

In TDM Mode, the two data-format options are supported as follows:

- TDM Mode—minimum slots. The ASP data format is configured to support two slots. This mode allows the BCLK rate to be as low as possible, equating to a minimum of 128 BCLK cycles per audio sample at a minimum sample rate of 64 Fs.

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- TDM Mode—maximum time slots. The ASP data format is configured to support the maximum number of time slots for the applicable BCLK rate. The mode is designed for the maximum BCLK rate (22.5792 MHz for sample rates of 44.1, 88.2, 176.4, and 352.8 kHz, or 24.576 MHz for sample rates of 16, 32, 48, 96, 192, and 384 kHz), enabling the maximum possible bandwidth on the ASP data bus to be shared with other devices.

The ASP configuration depends on the sample rate and the selected data format as described in Table 4-9.

Table 4-9. ASP Data Format

ASP Format [1]	ASP Sample Rate [2,3]	Time Slots per Frame [4]	BCLK Rate[5,6]
I²S, Left-Justified	16 kHz	2	BCLK ≥ 64×Fs[7]
	32 kHz		BCLK ≥ 64×Fs[8]
	44.1 kHz, 48 kHz		BCLK ≥ 64×Fs
	88.2 kHz, 96 kHz		BCLK ≥ 64×Fs
	176.4 kHz, 192 kHz		BCLK ≥ 64×Fs
	352.8 kHz, 384 kHz		BCLK ≥ 64×Fs
	Autodetect (16 kHz–192 kHz)		BCLK ≥ 64×Fs
TDM—minimum time slots	16 kHz		BCLK ≥ 64×Fs[7]
	32 kHz		BCLK ≥ 64×Fs[8]
	44.1 kHz, 48 kHz		BCLK ≥ 64×Fs
	88.2 kHz, 96 kHz		BCLK ≥ 64×Fs
	176.4 kHz, 192 kHz		BCLK ≥ 64×Fs
	352.8 kHz, 384 kHz		BCLK ≥ 64×Fs
	Autodetect (16 kHz–192 kHz)		BCLK ≥ 64×Fs
TDM—maximum time slots	16 kHz	16	BCLK ≥ 512×Fs[7]
	32 kHz		BCLK ≥ 512×Fs[8]
	44.1 kHz, 48 kHz		BCLK = 512×Fs
	88.2 kHz, 96 kHz	8	BCLK = 256×Fs
	176.4 kHz, 192 kHz	4	BCLK = 128×Fs
	352.8 kHz, 384 kHz	2	BCLK = 64×Fs
	Autodetect (16 kHz–192 kHz)	4	BCLK ≥ 128×Fs

1. The ASP format is selected using the CONFIG2 pin (in hardware control mode) or ASP_FORMAT (in software control mode).
2. The sample rate is selected using the CONFIG1 pin (in hardware control mode) or SAMPLE_RATE (in software control mode).
3. Sample rates 16 kHz–192 kHz are supported in hardware and software control modes; sample rate 384 kHz is supported in software control mode only.
4. Time slots per frame is the number of data-sample time slots supported on the DIN pin.
5. The BCLK rate must be a constant integer multiple of the sample rate (Fs).
6. In ASP Primary Mode (hardware control), the BCLK frequency is the minimum specified rate. In ASP Primary Mode (software control), the BCLK frequency is configured using ASP_BCLK_FREQ.
7. In ASP Primary Mode, the specified minimum BCLK frequency for 16 kHz sample rate is not supported. The available options correspond to 192×Fs, 384×Fs, 768×Fs, or 1536×Fs
8. In ASP Primary Mode, the specified minimum BCLK frequency for 32 kHz sample rate is not supported. The available options correspond to 96×Fs, 192×Fs, 384×Fs, or 768×Fs.

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The ASP data format in I²S, Left-Justified, and TDM interface modes as illustrated in Fig. 4-13 through Fig. 4-16. Refer to Table 4-9 for the applicable definition.

- If I²S data format is selected, the ASP supports audio channels 1–2 as shown in Fig. 4-13. The minimum BCLK rate is 64×Fs (where Fs is the sample rate). In ASP Primary Mode, the minimum BCLK rate of 64×Fs is not supported for sample rates of 16 kHz or 32 kHz. A higher BCLK frequency can be used, resulting in unused BCLK cycles between the LSB of one sample and the MSB of the next.

  The input data is provided on ASP_DIN.

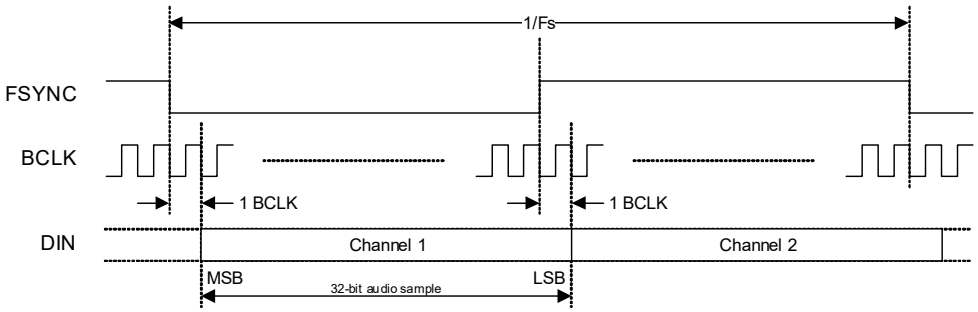

Figure 4-13. I²S Data Format

- If Left-Justified data format is selected, the ASP supports audio channels 1–2 as shown in Fig. 4-14. The minimum BCLK rate is 64×Fs (where Fs is the sample rate). In ASP Primary Mode, the minimum BCLK rate of 64×Fs is not supported for sample rates of 16 kHz or 32 kHz. A higher BCLK frequency can be used, resulting in unused BCLK cycles between the LSB of one sample and the MSB of the next.

  The input data is provided on ASP_DIN.

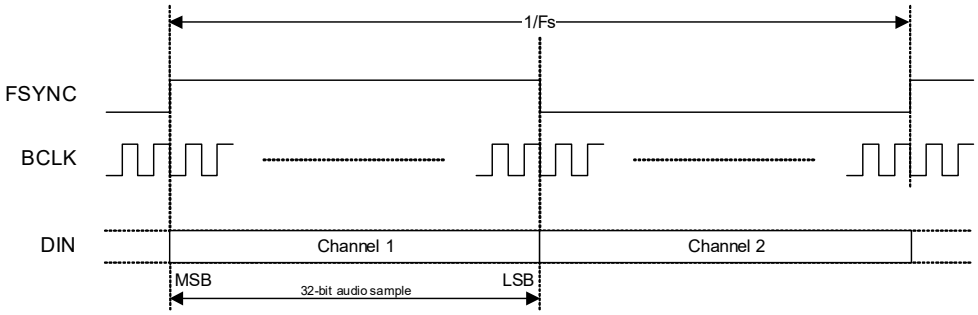

Figure 4-14. Left-Justified Data Format

- In TDM Mode, the FSYNC frame is configured for 2, 4, 8, or 16 slots as specified in Table 4-9.

  In 4-, 8-, and 16-slot modes, the slot assignment for audio channels 1–2 is selected using the CONFIG3 pin (in hardware control mode—see Section 4.2) or else using ASP_TDM_SLOT (in software control mode). In 2-slot modes, the default slot assignment (slots 0–1) should be selected.

  The BCLK rate is related to the sample rate (Fs) as described in Table 4-9. Where applicable, the BCLK rate can be higher than the stated minimum, resulting in additional unused BCLK cycles between the last slot in the frame and the start of the next frame.

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The input data is provided on ASP_DIN.

An example of the 4-slot TDM format in ASP Secondary Mode and in ASP Primary Mode with the FSYNC signal configured as a pulse is shown in Fig. 4-15. In this example, audio channels 1–2 occupy TDM slots 0–1 respectively.

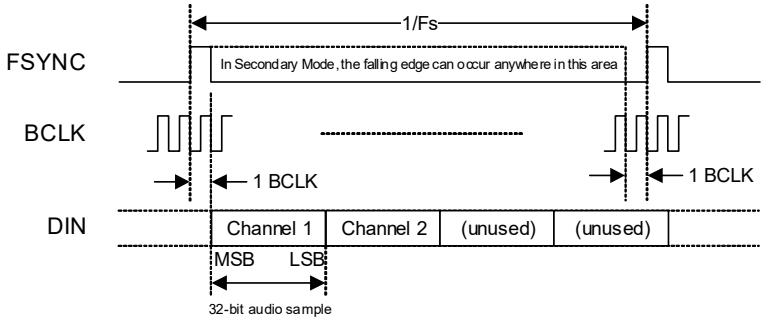

Figure 4-15. TDM Data Format, 4-Slot Example (FSYNC = Pulse)

An example of the 4-slot TDM format in ASP Primary Mode with the FSYNC signal configured as a square wave is shown in Fig. 4-16. In this example, audio channels 0 and 1 occupy TDM slots 0 and 1 in the high (Logic 1) phase of the FSYNC signal, TDM slot 0 and 1 in the low (Logic 0) phase of the FSYNC signal are unused.

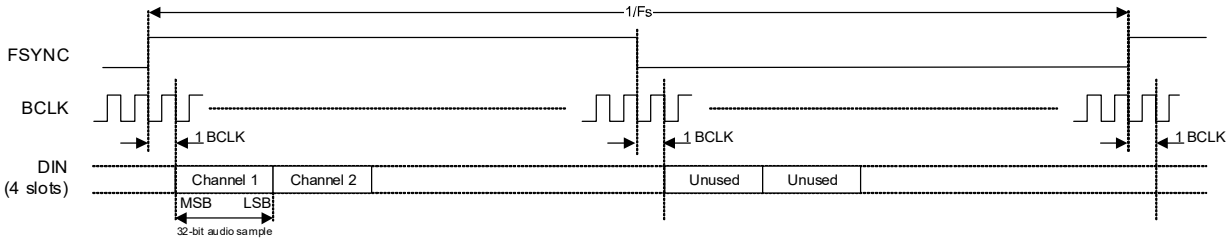

Figure 4-16. TDM Data Format, 4-Slot Example (FSYNC = Square Wave)

4.8 I2C/SPI Control Port

The CS4332BSE incorporates a control port, supporting I2C or SPI modes of operation; this is selected using CONFIG1, as described in Table 4-1. If the SPI control interface is required, it is recommended to use a pull-up resistor of 100 kΩ. In software control mode, the CS4332BSE is configured by writing to control registers using the control port.

The control port is automatically configured in I2C mode or SPI mode following the first valid I2C/SPI activity detected after power-on or hardware reset.

4.8.1 I2C Control Port

The I2C control port is supported using the following pins, which must be configured for the I2C function if required:

- CONFIG2/SPI_SDI/I2C_SDA
- CONFIG3/SPI_SDO/I2C_SCL

The CS4332BSE is a target device on the I2C bus—SCL is a clock input, while SDA is a bidirectional data pin. To allow arbitration of multiple targets (and/or multiple controllers) on the same interface, the CS4332BSE transmits Logic 1 by tristating the SDA pin, rather than pulling it high. An external pull-up resistor is required to pull the SDA line high so that the Logic 1 can be recognized by the controller.

In order to allow many devices to share a single two-wire control bus, every device on the bus has a unique 8-bit device address (this is not the same as the address of each register in the CS4332BSE). The LSB of the device address is the read/write bit; this bit is set to Logic 1 for read and Logic 0 for write.

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The I2C device address is configured using the CONFIG1 pin as described in Table 4-10.

Table 4-10. I2C Address Selection—CONFIG1 pin

Pin Configuration		I2C Address
Pull-up to VDD_IO1	0 kΩ	0x36 (write), 0x37 (read)
	4.7 kΩ	0x34 (write), 0x35 (read)
	22 kΩ	0x32 (write), 0x33 (read)
	100 kΩ	0x30 (write), 0x31 (read)

The host device indicates the start of data transfer with a high-to-low transition on SDA while SCL remains high. This indicates that a device address and subsequent address/data bytes follow. The CS4332BSE responds to the start condition and shifts in the next 8 bits on SDA (8-bit device address, including read/write bit, MSB first). If the device address received matches the device address of the CS4332BSE, the CS4332BSE responds by pulling SDA low on the next clock pulse (ACK). If the device address is not recognized or the R/W bit is set incorrectly, the CS4332BSE returns to the idle condition and waits for a new start condition.

If the device address matches the device address of the CS4332BSE, the data transfer continues. The controller indicates the end of data transfer with a low-to-high transition on SDA while SCL remains high. After receiving a complete address and data sequence the CS4332BSE returns to the idle state and waits for another start condition. If a start or stop condition is detected out of sequence at any point during data transfer (i.e., SDA changes while SCL is high), the device returns to the idle condition.

The I2C interface uses a 16-bit register address and 16-bit data words. The register address must be aligned to a 16-bit word boundary (i.e., the LSB must be 0). The full I2C message protocol also includes a device address, a read/write bit, and other signaling bits (see Fig. 4-17 and Fig. 4-18).

The CS4332BSE supports the following read and write operations:

- Single write
- Single read
- Multiple write
- Multiple read

Continuous (multiple) read and write modes allow register operations to be scheduled faster than is possible with single register operations. In these modes, the CS4332BSE automatically increments the register address after each data word. Successive data words can be input/output every two data bytes.

The I2C protocol for a single, 16-bit register write operation is shown in Fig. 4-17.

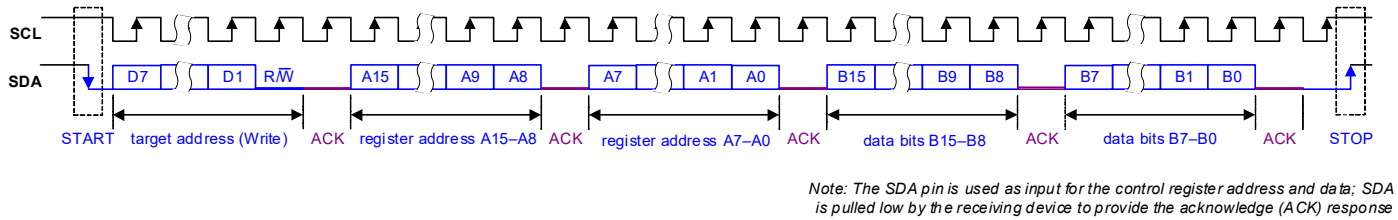

Figure 4-17. Control Interface I2C Register Write

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The I2C protocol for a single, 16-bit register read operation is shown in Fig. 4-18.

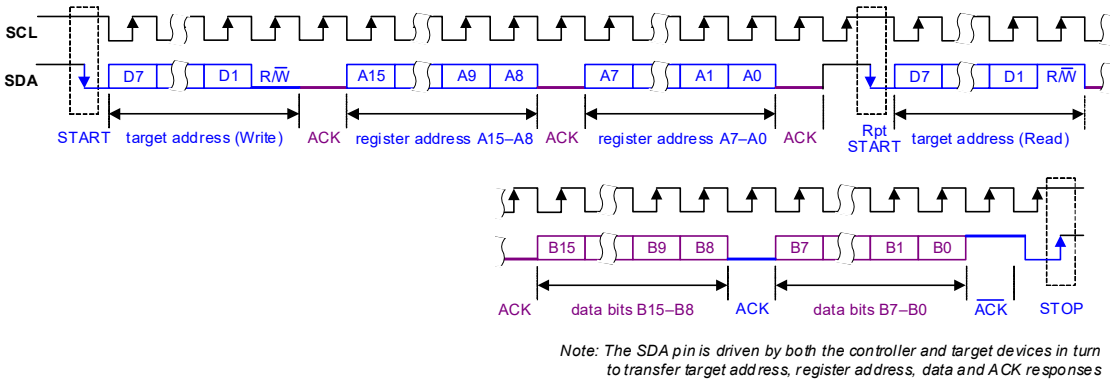

Figure 4-18. Control Interface I2C Register Read

The control interface also supports other register operations; the interface protocol for these operations is shown in Fig. 4-19 through Fig. 4-22. The terminology used in the following figures is detailed in Table 4-11.

Table 4-11. Control Interface (I2C) Terminology

Terminology	Description
S	Start condition
Sr	Repeated start
A	Acknowledge (SDA low)
$\overline{A}$	No Acknowledge (SDA high)
P	Stop condition
R/$\overline{W}$	Read/not Write: 0 = Write, 1 = Read
[White field]	Data flow from bus controller to CS4332BSE
[Gray field]	Data from CS4332BSE to bus controller

Fig. 4-19 shows a single register write to a specified address.

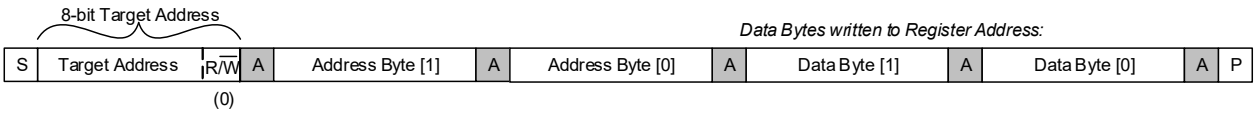

Figure 4-19. Single-Register Write to Specified Address

Fig. 4-20 shows a single register read from a specified address.

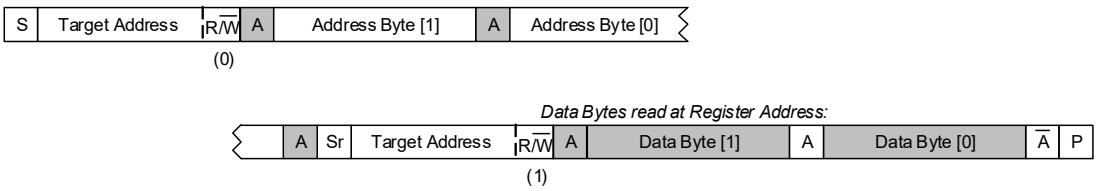

Figure 4-20. Single-Register Read from Specified Address

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Fig. 4-21 shows a multiple register write to a specified address.

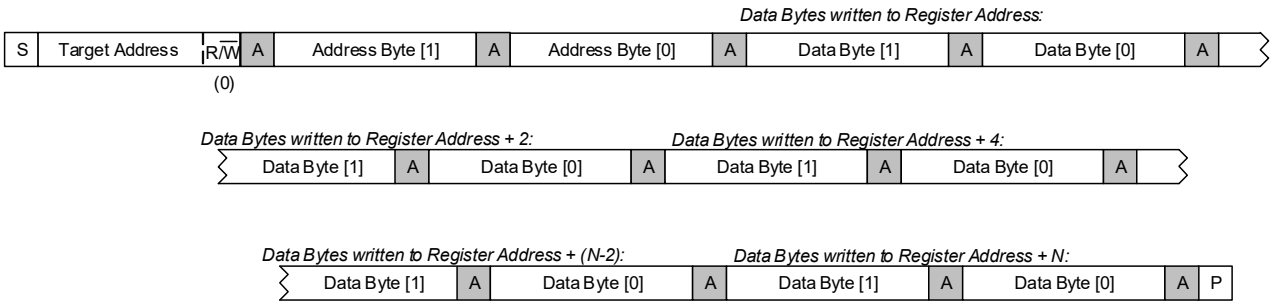

Figure 4-21. Multiple-Register Write to Specified Address

Fig. 4-22 shows a multiple register read from a specified address.

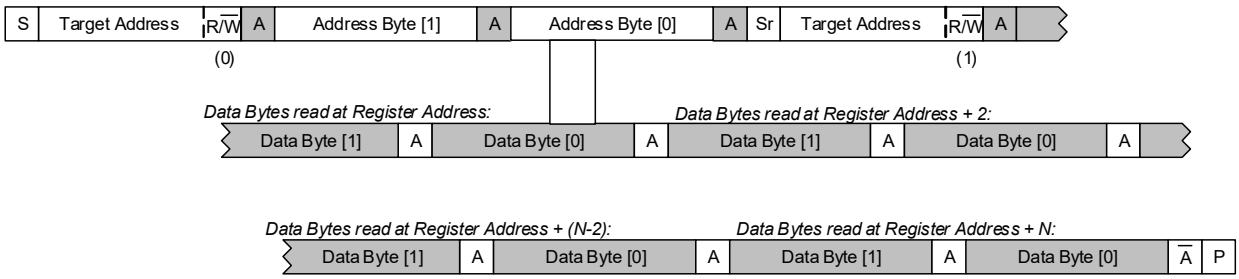

Figure 4-22. Multiple-Register Read from Specified Address

4.8.2 SPI Interface

The SPI interface is supported using the following pins, which must be configured for the SPI function if required:

- CONFIG1/$\overline{\text{SPI_CS}}$
- CONFIG2/SPI_SDI/I2C_SDA
- CONFIG3/SPI_SDO/I2C_SCL
- SPI_SCK

To ensure that the control port is inactive prior to use, $\overline{\text{SPI_CS}}$ must be deasserted (i.e., Logic 1) during device startup; $\overline{\text{RESET}}$ must remain asserted (i.e., Logic 0) until $\overline{\text{SPI_CS}}$ is deasserted (i.e., Logic 1), timing information is provided in Table 3-10.

The SDI (data-input) pin supports the following behavior:

- In write operations (R/$\overline{\text{W}}$ = 0), the SDI pin input is driven by the controlling device.
- In read operations (R/$\overline{\text{W}}$ = 1), the SDI pin is ignored following receipt of the valid register address.

The SDO (data-output) pin supports the following behavior:

- If $\overline{\text{CS}}$ is asserted (Logic 0), the SDO output is actively driven when outputting data and is high impedance at other times. If $\overline{\text{CS}}$ is not asserted, the SDO output is high impedance.
- The high-impedance state of the SDO output allows the pin to be shared with other peripheral devices.
- The output (SDO) data bit is available to the host device at the rising edge of SCK. See Table 3-13 for timing information.

The SPI interface uses a 15-bit register address and 16-bit data words. The full SPI message protocol also includes a read/write bit and a 16-bit padding phase (see Fig. 4-23 and Fig. 4-24).

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Continuous read and write modes enable multiple register operations to be scheduled faster than is possible with single register operations. In these modes, the CS4332BSE automatically increments the register address at the end of each data word, for as long as $\overline{CS}$ is held low and SCK is toggled. Successive data words can be input/output every 16 clock cycles.

The SPI protocol is shown in Fig. 4-23 and Fig. 4-24.

Fig. 4-23 shows a single register write to a specified address.

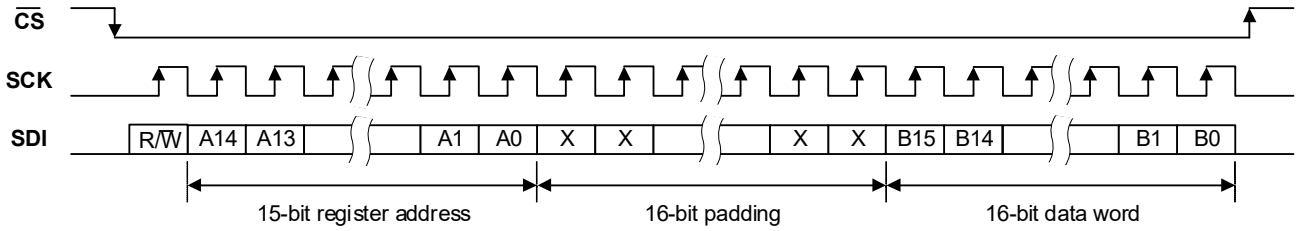

Figure 4-23. Control Interface SPI Register Write

Fig. 4-24 shows a single register read from a specified address.

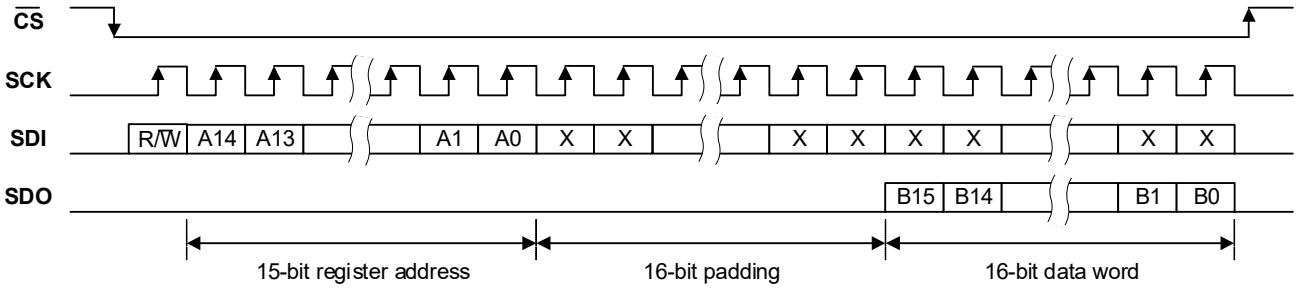

Figure 4-24. Control Interface SPI Register Read

Fig. 4-25 shows a multiple register write to a specified address.

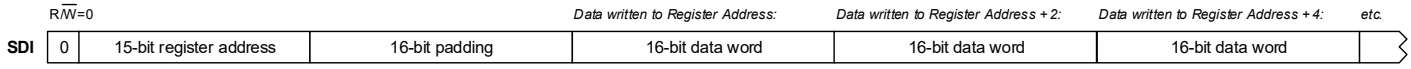

Figure 4-25. Multiple-Register Write to Specified Address

Fig. 4-26 shows a multiple register read from a specified address.

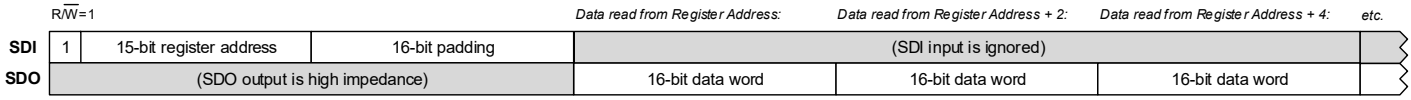

Figure 4-26. Multiple-Register Read from Specified Address

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4.9 Device ID

The device ID, and other associated data, can be read from the control fields listed in Table 4-12.

Table 4-12. Device ID

Label	Description
DEVID_0	Lower bytes of the Device ID
DEVID_1	Upper bytes of the Device ID
AREVID	All-layer device revision
MTLREVID	Metal-layer device revision

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5 Applications

5.1 Output Buffer Circuit

The CS4332BSE incorporates a high-performance sigma-delta current-mode DAC with integrated operational amplifiers for current-to-voltage conversion. External components for the current-to-voltage conversion and out-of-band filtering can be selected for flexible integration and to optimize dynamic range.

5.1.1 Typical Output Circuit

A typical output connection circuit is shown in Fig. 5-1. The circuit produces a 1 V_{RMS} single-ended output from a full-scale (0 dBFS) digital input.

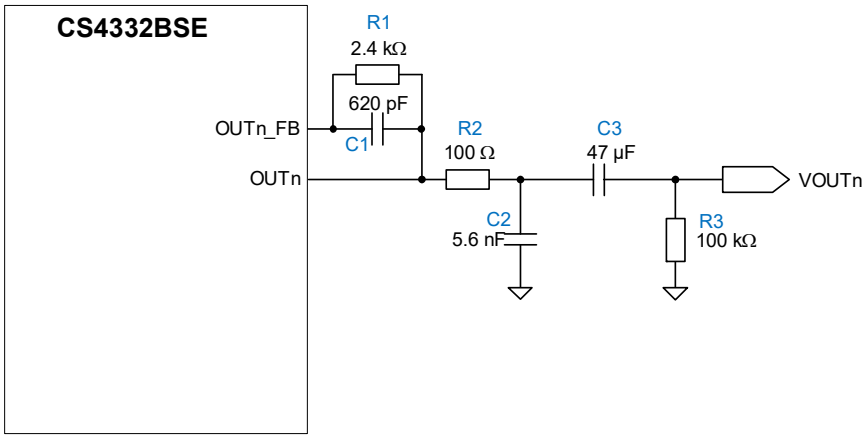

Figure 5-1. Typical Output Connection Circuit

The feedback resistor, R1 determines the full-scale single-ended output voltage; a maximum output voltage of 1 V_{RMS} is supported at the OUTn pins. R1 is calculated as follows:

$$R_1 = \frac{\text{Full-scale Output Voltage } (V_{RMS})}{0.418\ mA_{RMS}} = \frac{1}{0.418 \times 10^{-3}} = 2.4\ k\Omega$$

The filter is provided by the integrated operational amplifiers and associated feedback components C1 and R1. The objective is to provide a flat passband for the audio output bandwidth. The cut-off frequency of the filter is calculated as follows:

$$F_C = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi \times 2400 \times 620 \times 10^{-12}} = 107\ kHz$$

R2 and C2 create an output filter to reduce out-of-band noise of the output. The cut-off frequency of the filter is calculated as follows:

$$F_C = \frac{1}{2\pi R_2 C_2} = \frac{1}{2\pi \times 100 \times 5.6 \times 10^{-9}} = 284\ kHz$$

R3 and C3 form a high-pass filter, which removes the DC bias of the voltage output. The cut-off frequency of the filter is calculated as follows:

$$F_C = \frac{1}{2\pi R_3 C_3} = \frac{1}{2\pi \times 100 \times 10^3 \times 47 \times 10^{-6}} = 0.033\ Hz$$

Note: The cut-off frequency of the filter varies with the load on VOUTn.

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5.1.2 Alternative Output Circuits

The typical circuit shown in Fig. 5-1 is recommended for optimal performance. An example line driver circuit, designed for high-quality listening experience,is described in Section 5.1.2.1;specifications detailed in Section 3 are not applicable.

5.1.2.1 Example Active Line Driver Circuit

An example of an active line-driver circuit is shown in Fig. 5-2, the output connection circuit shown produces a 1 V_{RMS} output from a full-scale (0 dBFS) digital input.

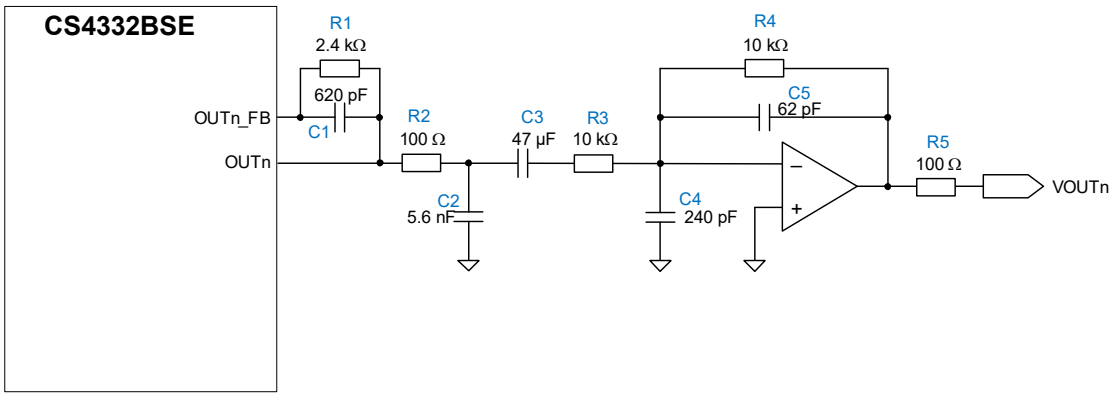

Figure 5-2. Example Active Line Driver Circuit

The feedback resistor, R1 determines the full-scale single-ended output voltage; a maximum output voltage of 1 V_{RMS} is supported at the OUTn pins. R1 is calculated as follows

$$R_1 = \frac{\text{Full-scale Output Voltage } (V_{RMS})}{0.418\ mA_{RMS}} = \frac{1}{0.418 \times 10^{-3}} = 2.4\ k\Omega$$

The filter is provided by the integrated operational amplifier and associated feedback components C1 and R1. The objective is to provide a flat passband for the audio output bandwidth. The cut-off frequency of the filter is calculated as follows:

$$F_C = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi \times 2400 \times 620 \times 10^{-12}} = 107\ kHz$$

R2 and C2 create an output filter to reduce the out-of-band noise of the output. The cut-off frequency of the filter is calculated as follows:

$$F_C = \frac{1}{2\pi R_2 C_2} = \frac{1}{2\pi \times 100 \times 5.6 \times 10^{-9}} = 284\ kHz$$

C3 removes the DC bias of the CS4332BSE output and forms a high-pass filter with R3. The cut-off frequency of the filter is calculated as follows:

$$F_C = \frac{1}{2\pi R_3 C_3} = \frac{1}{2\pi \times 10 \times 10^3 \times 47 \times 10^{-6}} = 0.34\ Hz$$

R3 and C4 create a low-pass filter. The cut-off frequency of the filter is calculated as follows:

$$F_C = \frac{1}{2\pi R_3 C_4} = \frac{1}{2\pi \times 10 \times 10^3 \times 240 \times 10^{-12}} = 66.3\ kHz$$

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R4 and C5 create a low-pass filter within the operational amplifier feedback loop. The cut-off frequency of the filter is calculated as follows:

$$F_C = \frac{1}{2\pi R_4 C_5} = \frac{1}{2\pi \times 10 \times 10^3 \times 62 \times 10^{-12}} = 256.7\ \text{kHz}$$

The gain of the output buffer is set by R3 and R4:

$$\text{Gain} = \frac{R_4}{R_3} = \frac{10 \times 10^3}{10 \times 10^3} = 1$$

R5 limits the output current; this ensures stability of the output.

5.1.3 Unused Output Pins

The typical output connection circuit (Fig. 5-1) provides a single-ended output. Where an output channel is not used, the unused output pin (OUTn) must be connected to its respective OUTn_FB pin, as illustrated in Fig. 5-3.

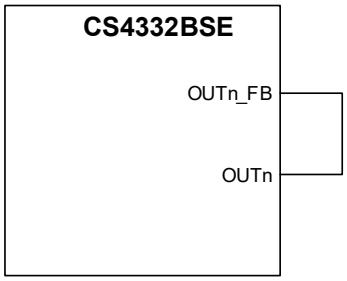

Figure 5-3. Unused Output Pin Connection

5.2 PCB Layout Guidelines

The recommended layout guidelines are provided in this section. Typical external components are described in Section 2.

5.2.1 General Layout Guidelines

The following general guidelines should be followed:

- Digital signals should be supported using a controlled 50 Ω characteristic impedance.
- Avoid routing digital signals between power planes on an adjacent layer.
- Avoid routing analog and digital signals next to each other.
- If a signal crosses another signal on an adjacent layer, they should cross perpendicularly to prevent coupling.
- Signals must not cross power-plane shapes or ground cut-offs on an adjacent layer.

5.2.2 Component Placement

The following guidelines on component placement should be followed:

- Power supply decoupling capacitors should be placed as close as possible to the CS4332BSE, with a strong connection to the ground plane.
- The voltage reference (DAC_VMID) capacitors and LDO filter (LDO_VD_FILT) capacitor should be placed close to the CS4332BSE, with a strong connection to the ground plane.

5.2.3 Ground Routing

The following guidelines are recommended for ground connection:

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- The ground paddle of the CS4332BSE should be connected to the ground plane with at least five vias.
- The ground paddle should not be connected directly to any pin.

5.2.4 VDD_A Routing

The following guidelines are recommended for the VDD_A supply:

- VDD_A1 and VDD_A2 should be star-connected to a 3.3 V power plane.
- Decoupling capacitors (0.01 µF and 4.7 µF) should be provided for each supply pin (VDD_A1 and VDD_A2), as shown in Section 2.

5.2.5 DAC_FILT Routing

The following guidelines are recommended for the DAC_FILT_P and DAC_FILT_N pins:

- Decoupling capacitors (22 µF) should be connected to DAC_FILT_P and DAC_FILT_N, as shown in Section 2.
- The DAC_FILT_P and DAC_FILT_N decoupling capacitors should be placed close to the CS4332BSE.
- The DAC_FILT_P decoupling capacitor should be connected to VDD_A1 as close as possible to the decoupling capacitors for VDD_A1.
- The DAC_FILT_N decoupling capacitor should be connected to the ground plane with a dedicated via.

5.3 Recommended Components

To achieve the specified performance characteristics, the choice of external components should observe the following recommendations:

- Capacitors should be stable dielectric types, such as C0G (NP0) or electrolytic.
- Resistors should be low value where possible, to minimize thermal noise.
- Low-noise operational amplifiers should be used, such as Texas Instruments OPA1656. The operational amplifiers should meet the minimum performance requirements noted in Table 5-1.

Table 5-1. Op-Amp Specification

Parameter	Specification
Input noise	<5 nV/√Hz
Unity gain bandwidth	>15 MHz
Slew rate	5 V/µs
Total harmonic distortion plus noise (THD+N)	<–128 dB

5.3.1 Crystal Component Selection

The crystal oscillator (see Section 4.4) uses an external crystal to generate the timing reference. Load capacitors are connected to the crystal as shown in Fig. 5-4. A series resistor (R_S) may also be required to configure the drive level for the selected crystal.

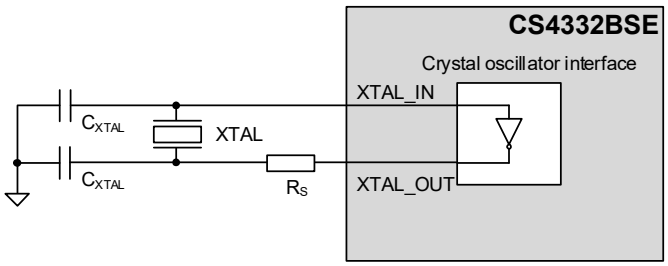

Figure 5-4. Crystal Oscillator Connection

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The suitability of the selected crystal is determined by whether the gain margin and drive level are within the valid operating limits of the crystal. The gain margin and drive level can be calculated as a function of the transconductance of the crystal interface.

The transconductance of the crystal interface is dependent on the VDD_IO2 operating voltage as described in Table 3-10.

The recommended sequence for crystal component selection is as follows:

1. **Crystal selection.** The CS4332BSE is compatible with a wide variety of crystal components, including the KC3225Z series of oscillators. Note that for a reference frequency of 45.1584 MHz a custom crystal may be required.
2. **Capacitor selection.** Capacitors should be selected according to the crystal manufacturer's specification for load capacitance (C_L). The recommended value for each C_{XTAL} capacitor is $2 \times C_L$.
3. **Series resistor.** In the first instance, assume the series resistor Rs is not required (0 Ω).
4. **Gain margin calculation.** The gain margin can be calculated from the transconductance of the crystal interface and the series resistor R_S, together with the crystal characteristics. If the required gain margin is less than 5, a different crystal selection must be made (Step 1).

   The gain margin is calculated as follows: $\text{Gain Margin} = \dfrac{\text{Transconductance}}{4 \times (ESR + R_S) \times (2\pi \times f_{XTAL})^2 \times (C_0 + C_L)^2}$

   where:

   Transconductance = transconductance of the crystal interface (S)

   ESR = equivalent series resistance (ESR) of the crystal (Ω)

   R_S = series resistance (Ω)

   f_{XTAL} = resonant frequency of the crystal (Hz)

   C_L = load capacitance of the crystal (F)

   C_0 = shunt capacitance of the crystal (F)
5. **Drive level calculation.** The drive level can be calculated using the crystal characteristics and the operating voltage. The operating voltage (peak voltage across the crystal) can be determined using measurement or else by simulation. If the drive level exceeds the maximum level for the crystal, adjust the series resistor R_S to meet the required specification. Increasing R_S results in a lower voltage across the crystal and a decrease in drive level.

   If the series resistor is adjusted, the gain margin must now be recalculated (Step 4). It is recommended to find the minimum series resistance that meets the required gain margin and drive level.

   The drive level (W) is calculated as follows: $\text{Drive Level} = 2 \times ESR \times (\pi \times f_{XTAL} \times V \times (C_L + C_0))^2$

   where:

   ESR = equivalent series resistance (ESR) of the crystal (Ω)

   f_{XTAL} = resonant frequency of the crystal (Hz)

   V = Peak voltage across the crystal (V)

   C_L = load capacitance of the crystal (F)

   C_0 = shunt capacitance of the crystal (F)

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The sequence for crystal component selection is illustrated in Fig. 5-5.

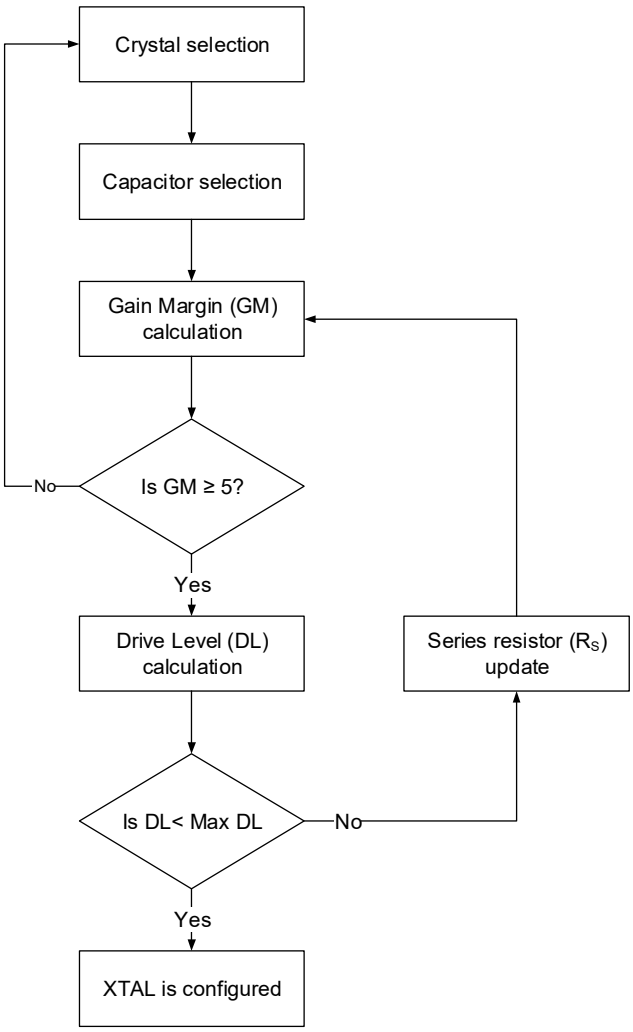

Figure 5-5. Crystal Oscillator Component Selection

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6 Register Quick Reference

This section gives an overview of the control port registers. Refer to the following bit definition tables for bit assignment information.

This register view is for the CS4332BSE.

- The register field default values are established upon the deassertion of the $\overline{\text{RESET}}$ pin or following soft reset.
- A "—" represents a reserved field/access type.
- The reserved field values must not be modified.
- The registers are 16 bits wide, and only word transactions are allowed.
- All visible fields are read/write except where indicated with the following shading:

Read/write access Read-only access Write-only access

Table 6-1. Block Base Addresses

Base Address	Block Name	Register Quick Reference	Register Description Reference
0x0000 0000	**DEVID**	Section 6.1	Section 7.1
0x0000 0040	**CONFIG**	Section 6.2	Section 7.2
0x0000 00C0	**OUTPUT_PATH**	Section 6.3	Section 7.3
0x0000 2000	**SIG_CTRL**	Section 6.4	Section 7.4

6.1 DEVID

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 0000	DEVID_0	DEVID_0															
p. 41		0	0	1	1	0	0	1	1	0	0	1	0	0	0	0	1
0x0000 0002	DEVID_1	DEVID_1															
p. 41		0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
0x0000 0004	REVID	—								AREVID				MTLREVID			
p. 41		0	0	0	0	0	0	0	0	1	0	1	1	0	0	0	0
0x0000 0022	SW_RESET	SW_RESET								—							
p. 42		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.2 CONFIG

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 0040	CLK_CFG	—		SYSCLK_FREQ	SYSCLK_SRC	—											
p. 42		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 0042	SAMPLE_RATE	—													SAMPLE_RATE		
p. 42		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0x0000 0044	CHIP_ENABLE	—															GLOBAL_EN
p. 42		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 0048	ASP_CFG	—									ASP_BCLK_INV	ASP_PRIMARY	—			ASP_BCLK_FREQ	
p. 43		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 0050	SIGNAL_PATH_CFG	—									ASP_FSYNC_TYPE	ASP_TDM_SLOT			ASP_FORMAT		
p. 43		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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6.3 OUTPUT_PATH

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 00C0	OUT_ENABLES	—							OUT_LOAD_CFG	—						OUT2_DAC_EN	OUT1_DAC_EN
p. 43		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 00C2	OUT_RAMP_SUM	—									OUT_RAMP_RATE_DEC			—	OUT_RAMP_RATE_INC		
p. 44		0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0
0x0000 00C4	OUT_DEEMPH	—														OUT_DEEMPH_FILT_SEL	OUT_DEEMPH_EN
p. 44		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 00CA	OUT_INV	—														OUT2_INV	OUT1_INV
p. 44		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
0x0000 00D0	OUT1_VOL_CTRL	OUT1_MUTE	—							OUT1_VOL							
p. 45		1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 00D2	OUT2_VOL_CTRL	OUT2_MUTE	—							OUT2_VOL							
p. 45		1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 00E0	OUT_VOL_UPDATE	—															OUT_VU
p. 45		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0000 00E4	SHUTDOWN_CTRL1	—															DAC_SHUTDOWN
p. 45		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

6.4 SIG_CTRL

Address	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x0000 2510	OUT_SIG_ACT_EN	—			OUT_EMA_TIME					—						OUT_SIG_ACT_EN	
p. 46		0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0
0x0000 2514	OUT1_SIG_ACT_THR	—											OUT1_SIG_ACT_THR				
p. 46		0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1
0x0000 2518	OUT2_SIG_ACT_THR	—											OUT2_SIG_ACT_THR				
p. 46		0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1

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7 Register Descriptions

This section describes each of the control port registers.

This register view is for the CS4332BSE.

- The register field default values are established upon the deassertion of the $\overline{\text{RESET}}$ pin or following soft reset.
- A "—" represents a reserved field/access type.
- The reserved field values must not be modified.
- The registers are 16 bits wide, and only word transactions are allowed.
- All visible fields are read/write except where indicated with the following shading:

Read/write access Read-only access Write-only access

7.1 DEVID

7.1.1 DEVID_0

Address: 0x0000 0000

RO	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DEVID_0															
Default	0	0	1	1	0	0	1	1	0	0	1	0	0	0	0	1

Bits	Name	Description
15:0	DEVID_0	This register indicates the lower bytes of Device ID CS4332BSE 0x0000–0x3320 = Reserved 0x3321 = (Default) CS4332BSE 0x3322–0xFFFF = Reserved

7.1.2 DEVID_1

Address: 0x0000 0002

RO	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DEVID_1															
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bits	Name	Description
15:0	DEVID_1	This register indicates the upper bytes of Device ID CS4332BSE 0x0000–0x0003 = Reserved 0x0004 = (Default) CS4332BSE 0x0005–0xFFFF = Reserved

7.1.3 REVID

Address: 0x0000 0004

RO	15…8	7	6	5	4	3	2	1	0
	—	AREVID				MTLREVID			
Default	0x00	1	0	1	1	0	0	0	0

Bits	Name	Description
15:8	—	Reserved
7:4	AREVID	This field indicates the all-layer device revision. 0x0–0xA = Reserved 0xB = (Default) Revision Bx 0xC–0xF = Reserved
3:0	MTLREVID	This field indicates the metal-layer device revision. 0x0 = (Default) Revision x0 0x1–0xF = Reserved

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7.1.4 SW_RESET

Address: 0x0000 0022

WO	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SW_RESET								—							
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:8	SW_RESET	Software Reset. Writing 0x5A triggers a reset. 0x00 = (Default) No action 0x01–0x59 = Reserved 0x5A = Software reset 0x5B–0xFF = Reserved
7:0	—	Reserved

7.2 CONFIG

7.2.1 CLK_CFG

Address: 0x0000 0040

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—		SYSCLK_FREQ	SYSCLK_SRC	—											
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:14	—	Reserved
13	SYSCLK_FREQ	System clock frequency. 0 = (Default) 24.576/22.5792 MHz 1 = 49.152/45.1584 MHz
12	SYSCLK_SRC	System clock source. If XTAL is selected, the MCLK is the output clock. 0 = (Default) MCLK input 1 = XTAL input
11:0	—	Reserved

7.2.2 SAMPLE_RATE

Address: 0x0000 0042

RW	15…8	7	6	5	4	3	2	1	0
	—	—					SAMPLE_RATE		
Default	0x00	0	0	0	0	0	0	0	1

Bits	Name	Description
15:3	—	Reserved
2:0	SAMPLE_RATE	Audio sample frequency. Note the sample rate must be integer-related to the system clock frequency. Auto-detect is only valid if sample rate = 16-192 kHz, and the ASP is in Secondary Mode. 000 = 32 kHz 001 = (Default) 48/44.1 kHz 010 = 96/88.2 kHz 011 = 192/176.4 kHz 100 = 384/352.8 kHz 101 = Reserved 110 = Auto-detect 111 = 16 kHz

7.2.3 CHIP_ENABLE

Address: 0x0000 0044

RW	15…8	7	6	5	4	3	2	1	0
	—	—							GLOBAL_EN
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:1	—	Reserved
0	GLOBAL_EN	Global enable. Set to 1 to configure and enable all functions. Clear to 0 to disable. Note the clocking and ASP control registers are only valid on the rising edge of GLOBAL_EN. It is recommended to select the disabled state (GLOBAL_EN=0) before writing to these registers.

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7.2.4 ASP_CFG

Address: 0x0000 0048

RW	15…8	7	6	5	4	3	2	1	0
	—	—	ASP_BCLK_INV	ASP_PRIMARY	—			ASP_BCLK_FREQ	
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:7	—	Reserved
6	ASP_BCLK_INV	ASP BCLK polarity. Selects the valid BCLK edge for data sampling. In non-inverted mode, DIN data is valid on BCLK rising edge. In inverted mode, DIN data is valid on BCLK falling edge. 0 = (Default) Non-inverted 1 = Inverted
5	ASP_PRIMARY	ASP Primary/Secondary Mode select. In ASP Primary Mode, BCLK and FSYNC are outputs. In ASP Secondary Mode, BCLK and FSYNC are inputs. 0 = (Default) Secondary Mode 1 = Primary Mode
4:2	—	Reserved
1:0	ASP_BCLK_FREQ	ASP BCLK frequency. The BCLK frequency must be high enough to support the required number of data bits at the selected sample rate. Only valid in ASP Primary Mode. Note the BCLK frequency is integer-related to the system clock frequency i.e., multiples of 3.072 MHz for 24.576 / 49.152 MHz system clock, or multiples of 2.8224 MHz for 22.5792 / 45.1584 MHz system clock. 00 = (Default) 3.072/2.8224 MHz 01 = 6.144/5.6448 MHz 10 = 12.288/11.2896 MHz 11 = 24.576/22.5792 MHz

7.2.5 SIGNAL_PATH_CFG

Address: 0x0000 0050

RW	15…8	7	6	5	4	3	2	1	0
	—	—	ASP_FSYNC_TYPE	ASP_TDM_SLOT			ASP_FORMAT		
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:7	—	Reserved
6	ASP_FSYNC_TYPE	Configure ASP_FSYNC as pulse or square wave (50% duty cycle) in TDM mode. Only applicable when ASP is in Primary Mode. 0 = (Default) FSYNC Pulse 1 = FSYNC Square Wave
5:3	ASP_TDM_SLOT	TDM slot select. Configures which TDM slots are used in TDM maximum-time-slots mode. 000 = (Default) Slots 0-1 001 = Slots 2-3 010 = Slots 4-5 011 = Slots 6-7 100 = Slots 8-9 101 = Slots 10-11 110 = Slots 12-13 111 = Slots 14-15
2:0	ASP_FORMAT	ASP data format. Selects how the audio samples are arranged within the FSYNC frame. 000 = (Default) I2S Mode 001 = Left-Justified Mode 010–101 = Reserved 110 = TDM Mode maximum time slots 111 = TDM Mode minimum time slots

7.3 OUTPUT_PATH

7.3.1 OUT_ENABLES

Address: 0x0000 00C0

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—							OUT_LOAD_CFG	—						OUT2_DAC_EN	OUT1_DAC_EN
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:9	—	Reserved
8	OUT_LOAD_CFG	Output driving configuration. 0 = (Default) 3k load 1 = 10k load

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Bits	Name	Description
7:2	—	Reserved
1	OUT2_DAC_EN	Channel 2 output enable. 0 = (Default) Disabled 1 = Enabled
0	OUT1_DAC_EN	Channel 1 output enable. 0 = (Default) Disabled 1 = Enabled

7.3.2 OUT_RAMP_SUM

Address: 0x0000 00C2

RW	15…8	7	6	5	4	3	2	1	0
	—	—	OUT_RAMP_RATE_DEC			—	OUT_RAMP_RATE_INC		
Default	0x00	0	0	1	0	0	0	1	0

Bits	Name	Description
15:7	—	Reserved
6:4	OUT_RAMP_RATE_DEC	DAC output volume decrease Ramp Rate (ms/6 dB), used for gain changes. This field should not be changed while a volume ramp is in progress. 000 = 0 ms 001 = 0.5 ms 010 = (Default) 1 ms 011 = 2 ms 100 = 4 ms 101 = 8 ms 110 = 15 ms 111 = 30 ms
3	—	Reserved
2:0	OUT_RAMP_RATE_INC	DAC output volume increase Ramp Rate (ms/6 dB), used for gain changes. This field should not be changed while a volume ramp is in progress. 000 = 0 ms 001 = 0.5 ms 010 = (Default) 1 ms 011 = 2 ms 100 = 4 ms 101 = 8 ms 110 = 15 ms 111 = 30 ms

7.3.3 OUT_DEEMPH

Address: 0x0000 00C4

RW	15…8	7	6	5	4	3	2	1	0
	—	—						OUT_DEEMPH_FILT_SEL	OUT_DEEMPH_EN
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:2	—	Reserved
1	OUT_DEEMPH_FILT_SEL	Deemphasis filter sample-rate selection. 0 = (Default) 44.1 kHz 1 = 48.0 kHz
0	OUT_DEEMPH_EN	Deemphasis filter enable. 0 = (Default) Deemphasis disabled 1 = Deemphasis enabled

7.3.4 OUT_INV

Address: 0x0000 00CA

RW	15…8	7	6	5	4	3	2	1	0
	—	—						OUT2_INV	OUT1_INV
Default	0x00	0	0	0	0	0	0	1	1

Bits	Name	Description
15:2	—	Reserved
1	OUT2_INV	Channel 2 DAC invert. 0 = No inversion 1 = (Default) DAC data invert
0	OUT1_INV	Channel 1 DAC invert. 0 = No inversion 1 = (Default) DAC data invert

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7.3.5 OUT1_VOL_CTRL

Address: 0x0000 00D0

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OUT1_MUTE	—							OUT1_VOL							
Default	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	OUT1_MUTE	DAC output Channel 1 mute. 0 = Unmute 1 = (Default) Mute
14:8	—	Reserved
7:0	OUT1_VOL	DAC output Channel 1 volume, –127.5 dB to 0 dB in 0.5 dB steps. 0x00 = (Default) 0.0 dB … 0x01 = –0.5 dB 0xFF = –127.5 dB

7.3.6 OUT2_VOL_CTRL

Address: 0x0000 00D2

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OUT2_MUTE	—							OUT2_VOL							
Default	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15	OUT2_MUTE	DAC output Channel 2 mute. 0 = Unmute 1 = (Default) Mute
14:8	—	Reserved
7:0	OUT2_VOL	DAC output Channel 2 volume, –127.5 dB to 0 dB in 0.5 dB steps. 0x00 = (Default) 0.0 dB … 0x01 = –0.5 dB 0xFF = –127.5 dB

7.3.7 OUT_VOL_UPDATE

Address: 0x0000 00E0

WO	15…8	7	6	5	4	3	2	1	0
	—	—							OUT_VU
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:1	—	Reserved
0	OUT_VU	Global output volume update trigger. 0 = (Default) No action 1 = Write 1 to trigger an update of all output volume/mute registers

7.3.8 SHUTDOWN_CTRL1

Address: 0x0000 00E4

RW	15…8	7	6	5	4	3	2	1	0
	—	—							DAC_SHUTDOWN
Default	0x00	0	0	0	0	0	0	0	0

Bits	Name	Description
15:1	—	Reserved
0	DAC_SHUTDOWN	DAC reference shutdown control. Can be used to minimize power consumption if all output paths are disabled. 0 = (Default) Enable DAC reference 1 = Shutdown DAC reference

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7.4 SIG_CTRL

7.4.1 OUT_SIG_ACT_EN

Address: 0x0000 2510

RW	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—				OUT_EMA_TIME				—						OUT_SIG_ACT_EN	
Default	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:13	—	Reserved
12:8	OUT_EMA_TIME	Signal activity detection level-detect EMA filter time constant. The time constant is defined in audio sample (1/fs) units. 0x00–0x09 = Reserved 0x0A = 1024 samples 0x0B = 2048 samples 0x0C = (Default) 4096 samples 0x0D = 8192 samples 0x0E = 16384 samples 0x0F = 32768 samples 0x10 = 65536 samples 0x11–0x1F = Reserved
7:2	—	Reserved
1:0	OUT_SIG_ACT_EN	Output signal activity detection enable. 00 = (Default) Disabled 01–10 = Reserved 11 = Enabled

7.4.2 OUT1_SIG_ACT_THR

Address: 0x0000 2514

RW	15…8	7	6	5	4	3	2	1	0
	—	—			OUT1_SIG_ACT_THR				
Default	0x00	0	0	0	0	1	0	0	1

Bits	Name	Description
15:5	—	Reserved
4:0	OUT1_SIG_ACT_THR	Signal activity detection level-detect threshold. 0x00–0x02 = Reserved 0x03 = –2 dBFS … 0x09 = (Default) –38 dBFS … 0x13 = –98 dBFS 0x14–0x1F = Reserved

7.4.3 OUT2_SIG_ACT_THR

Address: 0x0000 2518

RW	15…8	7	6	5	4	3	2	1	0
	—	—			OUT2_SIG_ACT_THR				
Default	0x00	0	0	0	0	1	0	0	1

Bits	Name	Description
15:5	—	Reserved
4:0	OUT2_SIG_ACT_THR	Signal activity detection level-detect threshold. 0x00–0x02 = Reserved 0x03 = –2 dBFS … 0x09 = (Default) –38 dBFS … 0x13 = –98 dBFS 0x14–0x1F = Reserved

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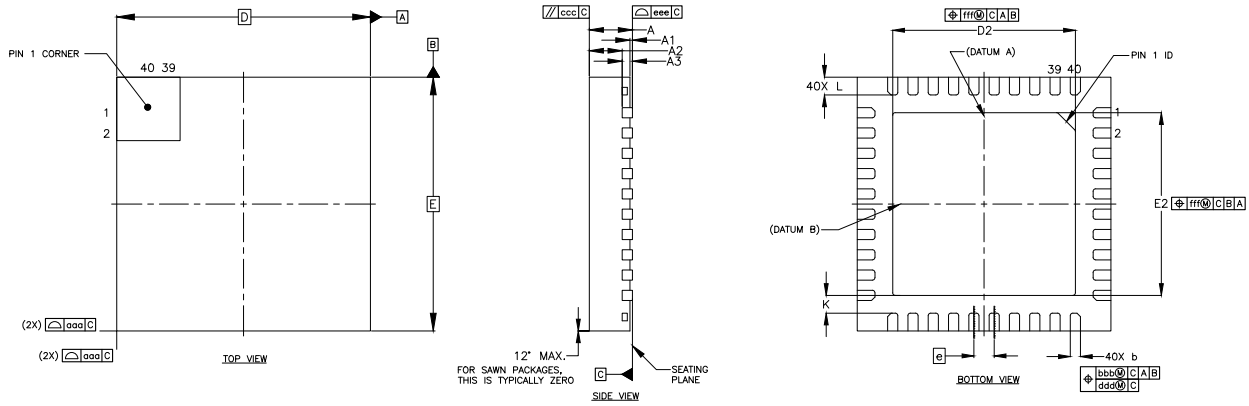
8 Thermal Characteristic

Table 8-1. Typical JEDEC Four-Layer, 2s2p Board Thermal Characteristics

Parameter	Symbol	QFN	Units
Junction-to-ambient thermal resistance	θ_{JA}	31.37	°C/W
Junction-to-board thermal resistance	θ_{JB}	17.18	°C/W
Junction-to-case (top) thermal resistance	θ_{JC}	115.39	°C/W
Junction-to-board thermal-characterization parameter	Ψ_{JB}	15.96	°C/W
Junction-to-package-top thermal-characterization parameter	Ψ_{JT}	2.75	°C/W

Notes:
- Natural convection at the maximum recommended operating temperature T_A (see Table 3-2)
- Four-layer, 2s2p PCB as specified by JESD51–9 and JESD51–11; dimensions: 101.5 x 114.5 x 1.6 mm
- Thermal parameters as defined by JESD51–12

9 Package Dimensions



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.80	0.85	0.90
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	–	0.65	–
L/F THICKNESS		A3	0.20 REF.		
LEAD WIDTH		b	0.15	0.20	0.25
BODY SIZE	X	D	5.0 BSC		
	Y	E	5.0 BSC		
LEAD PITCH		e	0.40 BSC		
EP SIZE	X	D2	3.50	3.60	3.70
	Y	E2	3.50	3.60	3.70
LEAD LENGTH		L	0.30	0.35	0.40
LEAD TO EP CLEARANCE		K	0.35 REF.		
PACKAGE EDGE TOLERANCE		aaa	0.10		
LEAD OFFSET		bbb	0.07		
		ddd	0.05		
MOLD FLATNESS		ccc	0.10		
COPLANARITY		eee	0.08		
EXPOSED PAD OFFSET		fff	0.10		

Figure 9-1. QFN Package Drawing

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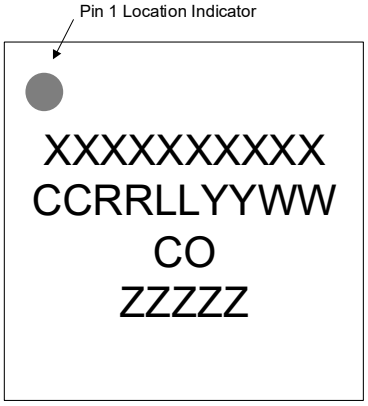
10 Package Marking

Figure 10-1. Package Marking



Top Side Brand
Line 1: Part number
Line 2: Package mark
Line 3: Country of origin (CO)
Line 4: Encoded wafer/device ID

Package Mark Fields
CC = Cirrus Logic Index Code
RR = Device revision code
LL = Lot sequence code
YY = Year of manufacture
WW = Work week of manufacture

11 Ordering Information

Table 11-1. Ordering Information

Product	Description	Package	Environmental Certifications	Grade	Temperature Range	Container	Orderable Part Number
CS4332BSE	High Performance Two-Channel Audio DAC	40-pin QFN	RoHS Compliant	Commercial	–40 to +85°C	Tray	CS4332BSE-DN
						Tape and Reel	CS4332BSE-DNR

12 References

- NXP Semiconductors, UM10204 Rev. 7, October 2021, *I2C-Bus Specification and User Manual*, https://www.nxp.com

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13 Revision History

Important: Please check www.cirrus.com or with your Cirrus Logic sales representative to confirm that you are using the latest revision of this document and to determine whether there are errata associated with this device.

Table 13-1. Revision History

Revision	Change
A3 OCT 2026	• Added Signal-Activity Detection to Features and General Description. • Updated Dynamic Range and THD+N values in Specifications. • Updated Pin Assignments and Descriptions (changes reflected throughout) (Section 1): —Renamed Pin 1 was GND_D, now NC; PAD was GND_A, now GND. —Changed LDO_VD_FILT power supply, was VDD_A1 now VDD_A2. —Updated table note related to ground connections • Updated Typical Connections Diagram (Section 2): —Renamed GND_D, GND_A, and PAD, as summarized above. —Renamed DAC_VMID and DAC_FILT_N decoupling connection, was GND_A, now GND (PAD). —Updated decoupling capacitor values on LDO_VD_FILT pins. —Updated note regarding clocking option configuration. —Added HGC pin names. —Added External Component Requirements (Table 2-1). • Updated Characteristics and Specifications (Section 3): —Updated bandwidth condition for performance measurements in Parameter Definitions table note (Table 3-1) —Removed GND_D from test conditions in all tables (Section 3). —Updated table note for Recommended Operating Conditions (Table 3-2). —Added Digital Core (LDO_VD_FILT) to Absolute Maximum Ratings (Table 3-3). —Added load to test conditions and updated THD_N and Load Resistance parameters in DAC Path Characteristics (Table 3-4). —Removed DC offset error specification in DAC Path Characteristics (Table 3-4). —Updated Group delay for Fast roll-off filter at F_S = 16 kHz in DAC Filter Characteristics (Table 3-5). —Updated Passband ripple parameter conditions for Balanced roll-off filter at F_S = 352.8 kHz or 384 kHz in DAC Filter Characteristics (Table 3-5). —Removed Phase deviation specification in DAC High Pass Filter Characteristics (Table 3-6). —Update test conditions and parameters in Device Power Consumption (Table 3-7). —Removed note related to DAC_FILT maximum output current in DC Characteristics (Table 3-9). —Updated VDD_IO2 POR threshold (V_{POR}) rising and falling maximum values in DC Characteristics (Table 3-9). —Removed reference to half-cycle mode in ASP timing in I2S and Left-Justified Modes parameter note in Switching Specifications—Audio Serial Port (ASP) (Table 3-11). —Updated VDD_IO in test conditions in Switching Specifications—SPI Control Port (Table 3-13). • Updated Functional Description (Section 4): —Clarified supported sample rates for different system clock frequencies (Section 4.2, Section 4.4, Section 4.4.1, Section 4.4.2, Section 4.7.1, Section 4.7.3). —Clarified external clock synchronization requirements in ASP Secondary Mode (Section 4.4.1, Section 4.4.2, Section 4.7.1). —Added signal-activity detection capability in Signal-Activity Detection (Section 4.6). • Updated Applications (Section 5): —Added PCB Layout Guidelines (Section 5.2). • Edited Registers (Section 7): —AREVID —OUTx_GPI_POL —OUTx_DIG_GAIN —OUT_SIG_ACT_EN —OUTx_SIG_ACT_THR —OUT_EMA_TIME
A2 MAY 2026	• Released for public distribution
A1 NOV 2025	• Initial version

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