# CS5312S

## *High Performance Two-Channel Audio ADC*

### Features

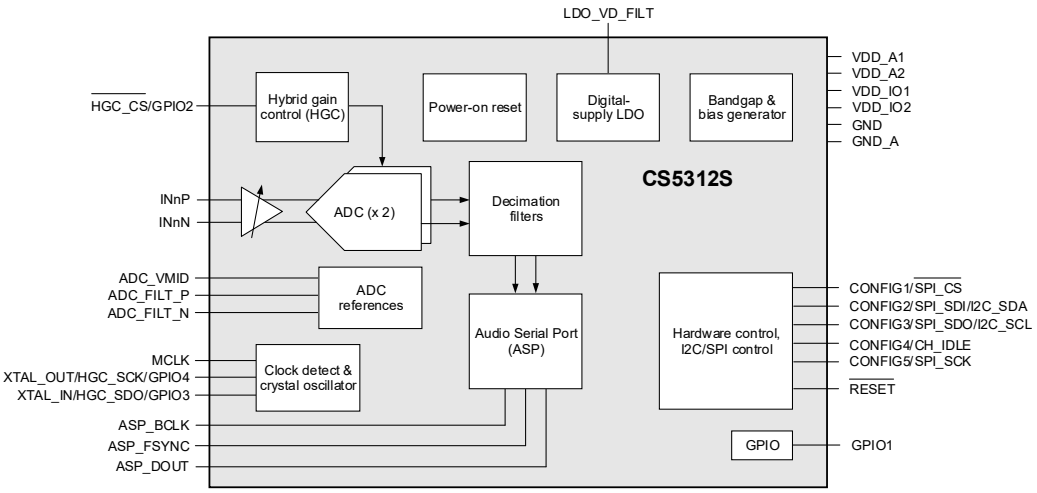
- High performance two-channel ADC
  - — Differential analog architecture
  - — High-resolution 32-bit digital design
  - — Low-latency digital filters and digital volume control
- Crystal oscillator interface
- Sample timing alignment across multiple devices
- Hybrid gain control (HGC)
  - — Synchronized control of external analog, and internal analog and digital gain
- Virtual passive attenuation device (PAD)
- Clip detection
- Signal-activity detection
- Audio serial port (ASP) sample rates up to 384 kHz
  - — I²S, left-justified, and TDM data formats
- Hardware and software control modes
  - — I²C control port up to 1 MHz
  - — SPI control port up to 24 MHz
  - — Hardware control with no host processor required
- Single-supply operation at 3.3 V
  - — Support for 1.8 V–3.3 V digital input/output
  - — Dual VDD_IO supplies support independent voltage domains for HGC and control interface
  - — 40-pin QFN package

### Specifications

- Advanced multibit sigma-delta ADC
  - — 116 dB dynamic range (A-weighted)
  - — –110 dB total harmonic distortion + noise (THD+N)
  - — 3.9/Fs group delay at 48 kHz sample rate (slow roll-off, minimum phase)
  - — 2 $V_{RMS}$ differential analog input
  - — High-pass filter

### Applications

- A/V receivers
- Digital mixing consoles
- Powered speakers
- Power amplifiers
- High-performance speakers and soundbars
- DAW interfaces
- Musical instruments
- Commercial audio systems

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## General Description

The CS5312S is a high-performance, 32-bit resolution, two-channel ADC. The CS5312S supports differential analog input and 32-bit digital output via the audio serial port (ASP) at sample rates up to 384 kHz. The ADC input path incorporates internal analog gain for signal amplification without additional noise or increased power consumption, minimizing external component requirements. Overall system efficiency and performance is enhanced by delivering superior input-referred noise performance and maintaining signal integrity between different applications.

The ADC provides differential architecture, optimized for high performance combined with low power consumption. The CS5312S uses a 5th-order, multibit sigma-delta modulator followed by digital filtering and decimation.

The CS5312S can be configured using a control interface supporting I²C™ and SPI™ modes of operation. The device can also be operated in hardware mode, using external resistors to select the required configuration. Multiple hardware-control options are supported, including system clocking source, ASP format, digital-filter selection, and sample rate.

The low-latency digital filters are optimized for the applicable sample rate. Fast and slow roll-off filters can be combined with minimum or linear phase responses to support the desired signal characteristics.

The CS5312S includes a virtual PAD function, to emulate a conventional PAD with minimal impact on the noise floor; this minimizes external component requirements leading to a more compact and efficient design. Zero-cross detection is used to synchronize the internal gain changes with zero points in the input signal, avoiding audible gain-change transients. An automatic PAD response feature is incorporated to prevent clipping of large signals at the ASP output.

A signal-activity detection function monitors the input signal on the ADC input paths to determine signal-activity level relative to configurable thresholds. The signal-activity level status (active or idle) is reported using a dedicated pin that can be monitored by the host to enable a quick and intelligent response to the audio environment, resulting in improved system-level efficiencies and enhanced overall user experience.

The CS5312S supports synchronized control of external analog gain associated with each ADC input path. The external gain settings can be configured through either the HGC serial interface or the GPIO pins. Dual VDD_IO supplies support independent voltage domains for the HGC function and the control interface. Updates to the external and internal gain settings are fully synchronized. A transient-masking function provides additional capability to ensure seamless operation across all signal levels.

The ASP supports operation in I²S, left-justified, and TDM data formats. Tristate control of the data-output pin allows multiple devices to operate on a shared bus.

Clocking for the CS5312S is provided by a separate clock source (MCLK) or else from the crystal oscillator. The ADC-sample timing is referenced to the ASP data frame, enabling time-aligned operation across multiple devices sharing a common data bus.

The CS5312S can be powered from a single 3.3 V supply. Digital output at 1.8 V logic levels is also possible using a separate external supply. The device combines high performance with low power consumption.

The CS5312S is available in a commercial-grade 0.4 mm pitch, 40-pin QFN package for operation from –40 °C to +85 °C.

See Section 11 for ordering information.



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# 1 Pin Assignments and Descriptions

## 1.1 40-Pin QFN (Top View, Through-Package)

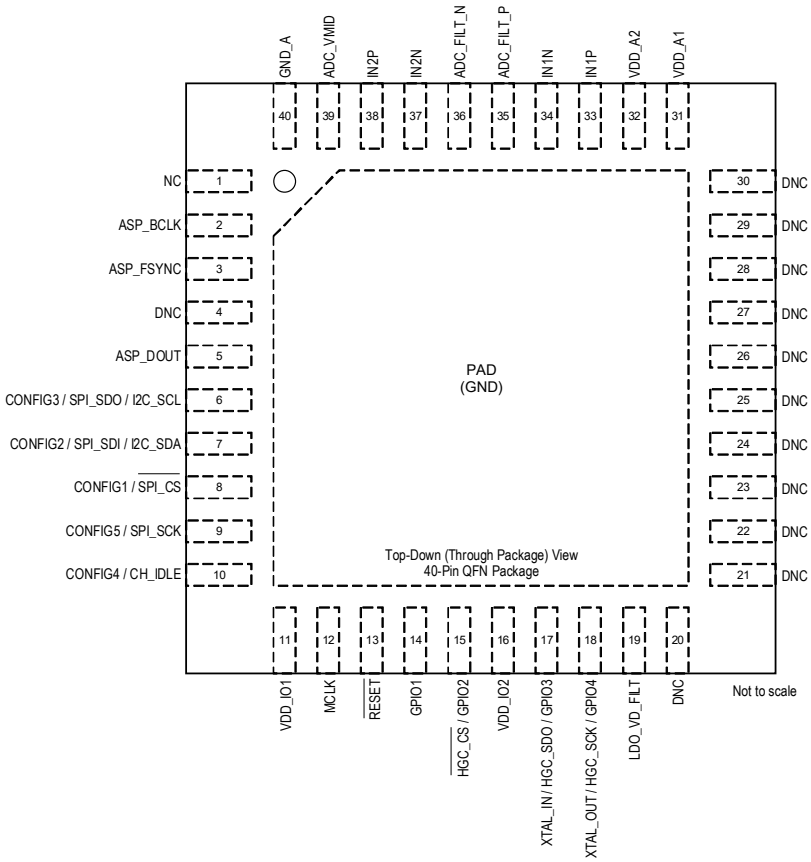


**Figure 1-1. QFN 40-Pin Diagram (Top View, Through Package)**

## 1.2 QFN Pin Descriptions

**Table 1-1. QFN Pin Descriptions**

| Pin Name | Pin # | Power Supply | I/O | Description |
|---|---|---|---|---|
| | | | | **Digital I/O** |
| ASP_BCLK | 2 | VDD_IO1 | I/O | Audio serial port bit clock. |
| ASP_DOUT | 5 | VDD_IO1 | O | Audio serial port data output. |
| ASP_FSYNC | 3 | VDD_IO1 | I/O | Audio serial port frame sync. |
| GPIO1 | 14 | VDD_IO2 | I/O | General-purpose input/output. |
| $\overline{\text{HGC_CS}}$/GPIO2 | 15 | VDD_IO2 | I/O | Hybrid gain control (HGC) chip select.<br>General-purpose input/output. |
| MCLK | 12 | VDD_IO1 | I/O | Main clock input/output. |
| $\overline{\text{RESET}}$ | 13 | VDD_IO1 | I | Hardware reset control (active low). |
| XTAL_IN/HGC_SDO/GPIO3 | 17 | VDD_IO2 | I/O | Input for an external crystal/HGC data output/General-purpose input/output. |
| XTAL_OUT/HGC_SCK/GPIO4 | 18 | VDD_IO2 | I/O | Output for an external crystal/HGC clock/General-purpose input/output. |
| | | | | **Analog I/O** |
| ADC_FILT_N | 36 | VDD_A2 | O | ADC external capacitor connection. |
| ADC_FILT_P | 35 | VDD_A2 | O | Connect ADC_FILT_P to VDD_A2 via a 1 Ω resistor. |


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**Table 1-1. QFN Pin Descriptions *(Cont.)***

| Pin Name | Pin # | Power Supply | I/O | Description |
|---|---|---|---|---|
| ADC_VMID | 39 | VDD_A2 | O | ADC mid-rail voltage reference output. |
| CONFIG1/$\overline{\text{SPI_CS}}$ | 8 | VDD_IO1 | I | Hardware control pins. |
| CONFIG2/SPI_SDI/I2C_SDA | 7 | VDD_IO1 | I/O | In software control mode, CONFIG1 to CONFIG3 and CONFIG5 support the SPI/I2C interface. |
| CONFIG3/SPI_SDO/I2C_SCL | 6 | VDD_IO1 | I/O | |
| CONFIG4/CH_IDLE | 10 | VDD_IO1 | I/O | In software control mode, CONFIG1 selects the I2C target address. |
| CONFIG5/SPI_SCK | 9 | VDD_IO1 | I | In software control mode, CONFIG4 supports Signal Activity Detection. |
| IN1N | 34 | VDD_A2 | I | Analog Input 1. |
| IN1P | 33 | VDD_A2 | I | |
| IN2N | 37 | VDD_A2 | I | Analog Input 2. |
| IN2P | 38 | VDD_A2 | I | |
| LDO_VD_FILT | 19 | VDD_A2 | O | LDO_D regulator external capacitor connection. |
| **Power Supplies** | | | | |
| VDD_A1 | 31 | — | — | Analog Supply 1. |
| VDD_A2 | 32 | — | — | Analog Supply 2. |
| VDD_IO1 | 11 | — | — | Digital I/O Supply 1. |
| VDD_IO2 | 16 | — | — | Digital I/O Supply 2. |
| GND | PAD | — | — | Ground [1]. |
| GND_A | 40 | — | — | Analog ground [1]. |
| **No Connect** | | | | |
| DNC | 4, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30 | — | — | Do not connect. |
| NC | 1 | — | — | No connection, it is recommended to connect to GND. |

1. The GND_A pin and the ground paddle must be tied to a common ground plane directly underneath the CS5312S. It is recommended that the GND_A pin and the ground paddle are connected separately to the ground plane; the ground paddle should be connected to the ground plane using at least five vias.


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## 1.3 Termination of Unused Pins

Table 1-2 shows the required termination for unused pins (i.e., if the functionality of the pin is not being used). Pins not listed must be connected as shown in the typical connection drawings (see Section 2).

**Table 1-2. Termination of Unused Pins**

| Name | Termination if unused |
|---|---|
| INnX [1] | Float |
| MCLK [2] | |
| CONFIG3/SPI_SDO/I2C_SCL | 10 kΩ pull-down to GND |
| CONFIG4/CH_IDLE | |
| CONFIG5/SPI_SCK | |
| GPIO1 | |
| $\overline{\text{HGC_CS}}$/GPIO2 | |
| XTAL_IN/HGC_SDO/GPIO3 | |
| XTAL_OUT/HGC_SCK/GPIO4 | |
| $\overline{\text{RESET}}$ | Connect to VDD_IO1 |

1. See Section 5.1.1 for requirements in case of single-ended input configurations.
2. If the system clock is provided by the crystal oscillator and an MCLK output is not required, MCLK should be left floating.

## 1.4 Electrostatic Discharge (ESD) Protection

ESD-sensitive device. The CS5312S is manufactured on a CMOS process. Therefore, it is generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken while handling and storing this device. This device is qualified to current JEDEC ESD protection standards.


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# 2 Typical Connections Diagram

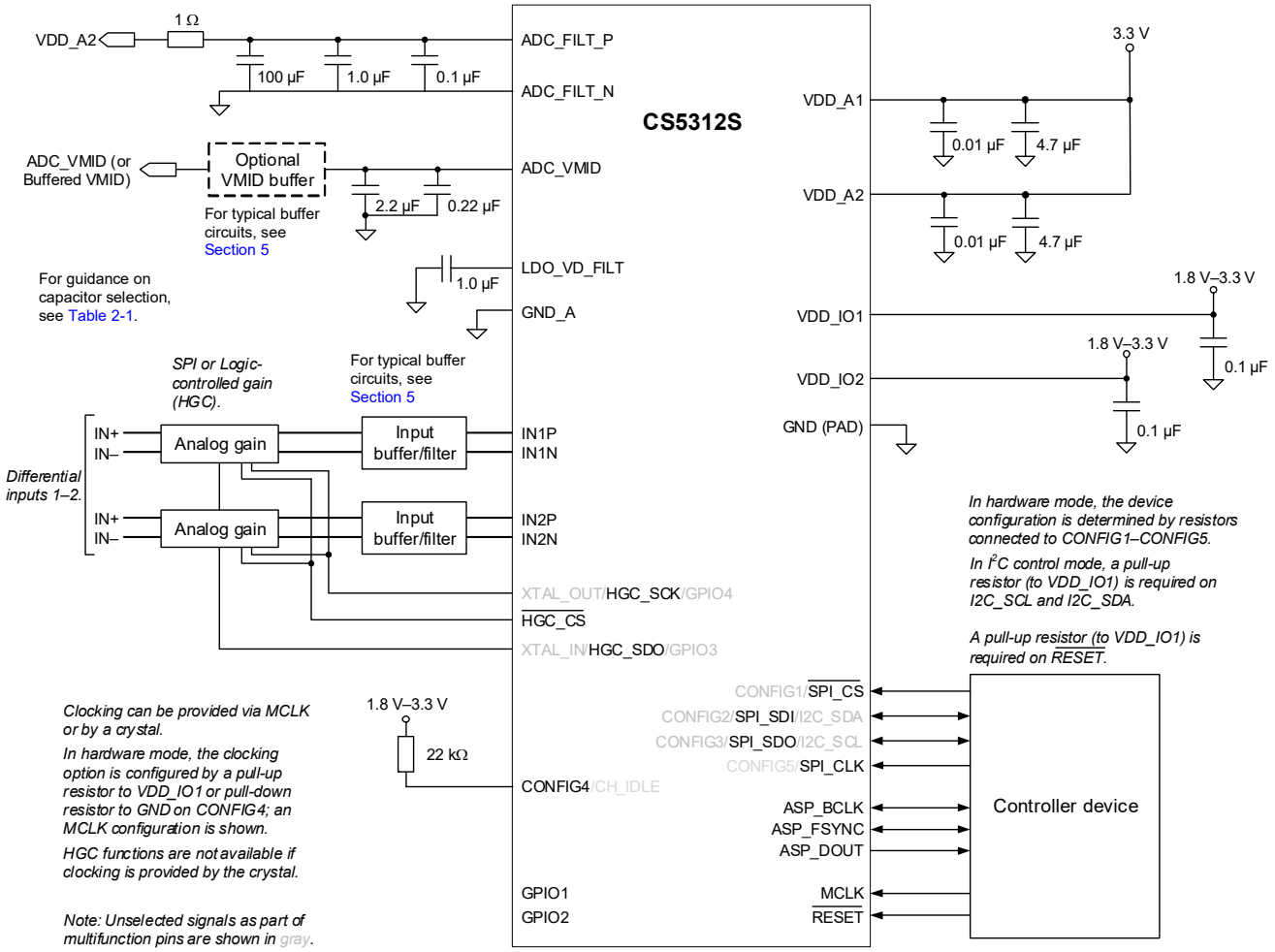


**Figure 2-1. Typical Connections**

Guidance on capacitor selection is provided in Table 2-1:

**Table 2-1. External Component Requirements**

| Connection | Capacitor | Requirements |
|---|---|---|
| LDO_VD_FILT | 1.0 µF ceramic | Must not derate below 0.8 µF at 1.2 V |
| ADC_VMID | 0.22 µF ceramic | Must not derate below 0.1 µF at 1.65 V |
| | 2.2 µF ceramic | Must not derate below 1.0 µF at 1.65 V |
| ADC_FILT | 0.47 µF ceramic | Must not derate below 0.22 µF at 3.3 V |
| | 4.7 µF ceramic | Must not derate below 2.2 µF at 3.3 V |
| | 100 µF electrolytic | Maximum leakage current 10 µA |
| VDD_A | 0.01 µF ceramic | — |
| | 4.7 µF ceramic | — |
| VDD_IO | 0.1 µF ceramic | — |


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# 3 Characteristics and Specifications

**Note:** Table 3-1 defines parameters as they are characterized in this section. Default register field configurations are used unless specified otherwise in the test conditions.

### Table 3-1. Parameter Definitions

| Parameter | Definition |
|---|---|
| Channel separation | The difference in level between the active channel (driven to maximum full scale output) and the measured signal level in the idle channel at the test signal frequency. The active channel is configured and supplied with an appropriate input signal to drive a full scale output, with signal measured at the output of the associated idle channel. |
| Common-mode rejection ratio (CMRR) | The ratio of a specified input signal (applied to both sides of a differential input), relative to the output signal that results from it. |
| Signal-to-noise ratio | The difference in level between the maximum full-scale output signal and the output with no input signal applied. |
| Dynamic range | The difference in level between the maximum full-scale output signal and the sum of all harmonic distortion products plus noise with a low-level input signal applied (an input signal level 60 dB below full scale is used). |
| Power-supply rejection ratio (PSRR) | The ratio of a specified power supply variation relative to the output signal that results from it. PSRR is measured under quiescent signal path conditions. |
| Total harmonic distortion plus noise (THD+N) | The ratio of the RMS sum of the harmonic distortion products plus noise in the specified bandwidth relative to the RMS amplitude of the fundamental (i.e., test frequency) output. |

**Note:** Unless specified otherwise, all performance measurements are for a 20 Hz to 20 kHz bandwidth.

### Table 3-2. Recommended Operating Conditions

Test conditions (unless specified otherwise): Ground = GND = GND_A = 0 V; voltages are with respect to ground.

| Parameter | | Symbol | Minimum | Maximum | Unit |
|---|---|---|---|---|---|
| DC power supply | Analog supply [1] | VDD_A1, VDD_A2 | 3.13 | 3.47 | V |
| | Digital I/O supply | VDD_IO1, VDD_IO2 | 1.71 | 3.63 | V |
| Supply ramp up/down (all supplies) | | $t_{PWR-UD}$ | 0.01 | 10 | ms |
| Ambient temperature | | $T_A$ | –40 | 85 | °C |

**Note:** Functionality and parametric performance is not guaranteed or implied outside of the limits in this table. Operation outside of these limits may adversely affect device reliability.

1. The VDD_A1 and VDD_A2 rails should be tied together and powered from a single supply. The associated power domain is referred to as VDD_A.

### Table 3-3. Absolute Maximum Ratings

Test conditions (unless specified otherwise in this table): Ground = GND = GND_A = 0 V; voltages are with respect to ground.

| Parameter | | Symbol | Minimum | Maximum | Unit |
|---|---|---|---|---|---|
| DC power supply | Analog supply [1] | VDD_A1, VDD_A2 | –0.3 | 4.32 | V |
| | Digital core | LDO_VD_FILT | –0.3 | 1.52 | V |
| | Digital I/O supply | VDD_IO1, VDD_IO2 | –0.3 | 4.32 | V |
| External voltage applied to digital input/output | VDD_IO1 logic pins<br>VDD_IO2 logic pins | $V_{INDI}$ | –0.3<br>–0.3 | VDD_IO1 + 0.3<br>VDD_IO2 + 0.3 | V<br>V |
| External voltage applied to analog inputs | | $V_{INAI}$ | –0.3 | VDD_A + 0.3 | V |
| Input current | digital input/output<br>analog inputs | $I_{IN}$ | —<br>— | ±10<br>±10 | mA<br>mA |
| Ambient operating temperature | | $T_A$ | –40 | +115 | °C |
| Junction operating temperature | | $T_J$ | –40 | +125 | °C |
| Storage temperature | | $T_{STG}$ | –65 | +150 | °C |

**Caution:** Stresses beyond “Absolute Maximum Ratings” levels may cause permanent damage to the device. These levels are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Table 3-2 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1. The VDD_A1 and VDD_A2 rails should be tied together and powered from a single supply. The associated power domain is referred to as VDD_A.


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### Table 3-4. ADC Path Characteristics

Test conditions (unless specified otherwise in this table): External components as shown in Fig. 2-1 incorporating the typical input circuit illustrated in Fig. 5-1; VDD_A = VDD_IO1 = VDD_IO2 = 3.3 V; Ground = GND = GND_A = 0 V; voltages are with respect to ground; $T_A$ = +25 ºC; 1 kHz sine wave test signal; Fs = 48 kHz, 32-bit audio data, MCLK = 24.576 MHz.

| Parameter | | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Input impedance (INnP to INnN) | internal analog gain = 0 dB | — | 12 | — | kΩ |
| | internal analog gain = 6 dB | — | 6 | — | kΩ |
| | internal analog gain = 12 dB | — | 3 | — | kΩ |
| Full-scale differential input signal level (INnP to INnN) [1] | 0 dBFS output | — | 2.0 | — | $V_{RMS}$ |
| SNR | A-weighted | 112 | 116 | — | dB |
| | unweighted | 109 | 113 | — | dB |
| Dynamic range [2] | A-weighted | — | 116 | — | dB |
| | unweighted | — | 113 | — | dB |
| THD+N [2] | –1 dBFS output | — | –110 | –99 | dB |
| | –20 dBFS output | — | –92 | — | dB |
| | –60 dBFS output | — | –52 | — | dB |
| Input-referred noise (A-weighted) | internal analog gain = 0 dB | — | 3.55 | 4.97 | $\mu V_{RMS}$ |
| | internal analog gain = 6 dB | — | 2.51 | 3.52 | $\mu V_{RMS}$ |
| | internal analog gain = 12 dB | — | 1.78 | 2.49 | $\mu V_{RMS}$ |
| CMRR | 100 mV (peak-peak) 1 kHz | — | 80 | — | dB |
| Channel separation | | — | 110 | — | dB |
| Interchannel phase deviation | | — | 0.03 | — | degree |
| Interchannel gain deviation | | — | 0.1 | — | dB |
| Gain drift | | — | ±100 | — | ppm/°C |
| PSRR (VDD_A) | 100 mV (peak-peak) 1 kHz sine wave | — | 65 | — | dB |

1. The full-scale input signal level is also the maximum analog input level, before clipping occurs. A sinusoidal input signal is assumed. Full-scale input signal level scales with VDD_A.
2. Performance may be affected by the input buffer, a typical input buffer circuit is illustrated in Section 5.1.


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### Table 3-5. ADC Filter Characteristics

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO1 = VDD_IO2 = 3.3 V; Ground = GND = GND_A = 0 V; voltages are with respect to ground; $T_A$ = +25 ºC; 1 kHz sine wave test signal, 32-bit audio data.

| Parameter | | | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| Fs = 16 kHz | Fast roll-off | Passband | to –3 dB corner | — | — | 0.47 | Fs |
| | | Passband ripple | f ≤ 0.45 Fs | –0.092 | — | 0.092 | dB |
| | | Stopband attenuation | f ≥ 0.55 Fs | 98 | — | — | dB |
| | | Group delay [1] | linear phase | — | 20.5/Fs | — | s |
| | | | minimum phase | — | 4.1/Fs | — | s |
| Fs = 32 kHz | Fast roll-off | Passband | to –3 dB corner | — | — | 0.47 | Fs |
| | | Passband ripple | f ≤ 0.45 Fs | –0.092 | — | 0.092 | dB |
| | | Stopband attenuation | f ≥ 0.55 Fs | 98 | — | — | dB |
| | | Group delay [1] | linear phase | — | 20.5/Fs | — | s |
| | | | minimum phase | — | 4.1/Fs | — | s |
| Fs = 44.1 kHz or 48 kHz | Fast roll-off | Passband | to –3 dB corner | — | — | 0.48 | Fs |
| | | Passband ripple | f ≤ 0.46 Fs | –0.011 | — | 0.011 | dB |
| | | Stopband attenuation | f ≥ 0.54 Fs | 98 | — | — | dB |
| | | Group delay [1] | linear phase | — | 27.6/Fs | — | s |
| | | | minimum phase | — | 4.0/Fs | — | s |
| | Slow roll-off | Passband | to –3 dB corner | — | — | 0.46 | Fs |
| | | Passband ripple | f ≤ 0.42 Fs | –0.099 | — | 0.099 | dB |
| | | Stopband attenuation | f ≥ 0.58 Fs | 96 | — | — | dB |
| | | Group delay [1] | linear phase | — | 13.3/Fs | — | s |
| | | | minimum phase | — | 3.9/Fs | — | s |
| Fs = 88.2 kHz or 96 kHz | Fast roll-off | Passband | to –3 dB corner | — | — | 0.48 | Fs |
| | | Passband ripple | f ≤ 0.45 Fs | –0.006 | — | 0.006 | dB |
| | | Stopband attenuation | f ≥ 0.55 Fs | 111 | — | — | dB |
| | | Group delay [1] | linear phase | — | 32.3/Fs | — | s |
| | | | minimum phase | — | 6.3/Fs | — | s |
| | Slow roll-off | Passband | to –3 dB corner | — | — | 0.43 | Fs |
| | | Passband ripple | f ≤ 0.27 Fs | –0.011 | — | 0.011 | dB |
| | | Stopband attenuation | f ≥ 0.77 Fs | 103 | — | — | dB |
| | | Group delay [1] | linear phase | — | 7.0/Fs | — | s |
| | | | minimum phase | — | 4.1/Fs | — | s |
| Fs = 176.4 kHz or 192 kHz | Fast roll-off | Passband | to –3 dB corner | — | — | 0.47 | Fs |
| | | Passband ripple | f ≤ 0.43 Fs | –0.009 | — | 0.009 | dB |
| | | Stopband attenuation | f ≥ 0.57 Fs | 99 | — | — | dB |
| | | Group delay [1] | linear phase | — | 19.1/Fs | — | s |
| | | | minimum phase | — | 5.2/Fs | — | s |
| | Slow roll-off | Passband | to –3 dB corner | — | — | 0.29 | Fs |
| | | Passband ripple | f ≤ 0.12 Fs | –0.010 | — | 0.010 | dB |
| | | Stopband attenuation | f ≥ 0.67 Fs | 99 | — | — | dB |
| | | Group delay [1] | linear phase | — | 6.4/Fs | — | s |
| | | | minimum phase | — | 4.2/Fs | — | s |
| Fs = 352.8 kHz or 384 kHz | Fast roll-off | Passband | to –3 dB corner | — | — | 0.48 | Fs |
| | | Passband ripple | f ≤ 0.43 Fs | –0.010 | — | 0.010 | dB |
| | | Stopband attenuation | f ≥ 0.57 Fs | 100 | — | — | dB |
| | | Group delay [1] | linear phase | — | 23.8/Fs | — | s |
| | | | minimum phase | — | 7.5/Fs | — | s |
| | Slow roll-off | Passband | to –3 dB corner | — | — | 0.34 | Fs |
| | | Passband ripple | f ≤ 0.06 Fs | –0.010 | — | 0.010 | dB |
| | | Stopband attenuation | f ≥ 0.94 Fs | 129 | — | — | dB |
| | | Group delay [1] | linear phase | — | 5.8/Fs | — | s |
| | | | minimum phase | — | 4.7/Fs | — | s |

1. Group delay is measured from the time at which a signal is presented on the input pins (INnP/INnN) to the time of the first data bit of the corresponding FSYNC frame being output on the ASP_DOUT pin.


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### Table 3-6. ADC High-Pass Filter (HPF) Characteristics

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO1 = VDD_IO2 = 3.3 V; Ground = GND = GND_A =0 V; voltages are with respect to ground; $T_A$ = +25 ºC; 1 kHz sine wave test signal; Fs = 48 kHz, 32-bit audio data.

| Parameter | | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Passband | –0.01 dB corner | — | 19 | — | Hz |
| | –3 dB corner | — | 1 | — | Hz |
| Filter settling time | | — | 0.4 | — | s |

### Table 3-7. Device Power Consumption

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO1 = VDD_IO2 = 3.3 V; Ground = GND = GND_A = 0 V; voltages are with respect to ground; $T_A$ = +25 ºC; 1 kHz sine wave test signal; ASP Secondary Mode; Load capacitance (ASP_DOUT) = 20 pF; Fs = 48 kHz, 32-bit audio data.

| Use Configuration | | Typical Current (mA) | | | Total Power (mW) |
|---|---|---|---|---|---|
| | | $I_{VDD_A}$ | $I_{VDD_IO1}$ | $I_{VDD_IO2}$ | |
| Reset | $\overline{RESET}$ = Logic 0 | 0.24 | 0.08 | 0.001 | 1.06 |
| Two ADC channels enabled | | 14 | 0.8 | 0.001 | 48.84 |

### Table 3-8. Digital Interface Specifications and Characteristics

Test conditions (unless specified otherwise in this table): Ground = GND = GND_A = 0 V; voltages are with respect to ground; $T_A$ = +25 ºC.

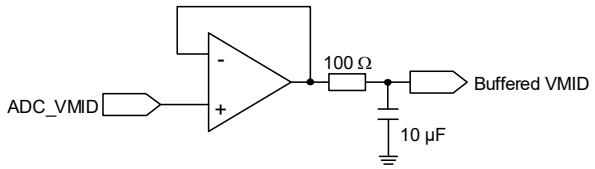
| Parameter | | Symbol | Minimum | Maximum | Unit |
|---|---|---|---|---|---|
| Input leakage current (per pin) | | $I_{IN}$ | — | ±10 | µA |
| Input capacitance (per pin) | | $C_{IN}$ | — | 5 | pF |
| Digital I/O (VDD_IO1 logic pins; see Section 1) | High-level output | $V_{OH}$ | 0.9×VDD_IO1 | — | V |
| | Low-level output | $V_{OL}$ | — | 0.1×VDD_IO1 | V |
| | High-level input | $V_{IH}$ | 0.7×VDD_IO1 | — | V |
| | Low-level input | $V_{IL}$ | — | 0.3×VDD_IO1 | V |
| Digital I/O (VDD_IO2 logic pins; see Section 1) | High-level output | $V_{OH}$ | 0.9×VDD_IO2 | — | V |
| | Low-level output | $V_{OL}$ | — | 0.1×VDD_IO2 | V |
| | High-level input | $V_{IH}$ | 0.7×VDD_IO2 | — | V |
| | Low-level input | $V_{IL}$ | — | 0.3×VDD_IO2 | V |

### Table 3-9. DC Characteristics

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO1 = VDD_IO2 = 3.3 V; Ground = GND = GND_A = 0 V; voltages are with respect to ground; $T_A$ = +25 ºC.

| Parameter | | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| LDO_VD_FILT | Nominal voltage | — | 1.2 | — | V |
| ADC_FILT | Nominal voltage | — | 3.3 | — | V |
| ADC_VMID [1] | Nominal voltage | — | 1.65 | — | V |
| | Maximum output current | — | 0.01 | — | mA |
| VDD_A power-on reset (POR) threshold ($V_{POR}$) | VDD_A rising | 2.0 | — | 2.8 | V |
| | VDD_A falling | 2.0 | — | 2.8 | V |
| VDD_IO1 power-on reset (POR) threshold ($V_{POR}$) | VDD_IO1 rising | 1.08 | — | 1.58 | V |
| | VDD_IO1 falling | 0.99 | — | 1.43 | V |
| VDD_IO2 power-on reset (POR) threshold ($V_{POR}$) | VDD_IO2 rising | 0.45 | — | 0.77 | V |
| | VDD_IO2 falling | 0.45 | — | 0.77 | V |

1. The output current (arising from capacitor leakage and the input-buffer circuit) must be less than the maximum output current of the ADC_VMID pin. If a larger current is required, an external ADC_VMID buffer should be used. A buffer can be provided using a standard op-amp (noise voltage < 5 nV/√Hz, input current < 10 µA), an example circuit is as follows.





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### Table 3-10. Switching Specifications—Reset and Clock References

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO1 = VDD_IO2 = 3.3 V; Ground = GND = GND_A = 0 V; voltages are with respect to ground; $T_A$ = +25 ºC.

| Parameter | | Symbol | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| Reset | $\overline{\text{RESET}}$ low (logic 0) pulse width | $t_{RLPW}$ | 1 | — | — | ms |
| | $\overline{\text{RESET}}$ rising edge to control port active | $t_{IRS}$ | — | — | 5 | ms |
| MCLK input | MCLK frequency | $f_{MCLK}$ | —<br>— | 24.576<br>22.5792 | —<br>— | MHz<br>MHz |
| | MCLK duty cycle | $D_{MCLK}$ | 45 | — | 55 | % |
| | MCLK frequency tolerance | — | –1 | — | 1 | % |
| MCLK output | MCLK frequency | $f_{MCLK}$ | —<br>— | 24.576<br>22.5792 | —<br>— | MHz<br>MHz |
| | MCLK duty cycle | $D_{MCLK}$ | 45 | — | 55 | % |
| | MCLK frequency accuracy | — | –1 | — | 1 | % |
| Crystal | Oscillator frequency | $f_{XTAL}$ | —<br>— | 24.576<br>22.5792 | —<br>— | MHz<br>MHz |
| | Interface transconductance VDD_IO2 = 3.3 V<br>VDD_IO2 = 1.8 V | — | —<br>— | 26<br>43 | —<br>— | mS<br>mS |


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### Table 3-11. Switching Specifications—Audio Serial Port (ASP)

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO2 = 3.3 V; Ground = GND = GND_A = 0 V; voltages are with respect to ground; input timings are measured at $V_{IL}$ and $V_{IH}$ thresholds, output timings are measured at $V_{OL}$ and $V_{OH}$ thresholds for VDD_IO1 logic (as specified in Table 3-8); $T_A$ = 25 °C.

| Parameter [1,2,3,4,5] | | | Symbol | Minimum | Maximum | Unit |
|---|---|---|---|---|---|---|
| Secondary Mode, VDD_IO1 = 3.3 V | ASP_FSYNC input sample/frame rate | | Fs | 16 | 384 | kHz |
| | ASP_FSYNC pulse width | | $t_{HI:FSYNC}$ | $1/f_{ASP_BCLK}$ | — | ns |
| | ASP_BCLK frequency | | $f_{BCLK}$ | 1.024 | 24.576 | MHz |
| | ASP_BCLK high period | | $t_{HI:BCLK}$ | 18 | — | ns |
| | ASP_BCLK low period | | $t_{LO:BCLK}$ | 18 | — | ns |
| | ASP_FSYNC setup time before ASP_BCLK latching edge | | $t_{SU:FSYNC}$ | 5 | — | ns |
| | ASP_FSYNC hold time after ASP_BCLK latching edge | | $t_{H:FSYNC}$ | 5 | — | ns |
| | ASP_DOUT delay after ASP_BCLK launching edge | half-cycle mode, load = 50 pF<br>full-cycle mode, load = 150 pF | $t_{D:BCLK–DOUT}$ | 0<br>0 | 10<br>12 | ns<br>ns |
| | ASP_DOUT Hi-Z delay after ASP_BCLK latching edge | half-cycle mode, load = 50 pF<br>full-cycle mode, load = 150 pF | $t_{DLY:HiZ}$ | 0<br>0 | 9<br>9 | ns<br>ns |
| | ASP_DOUT delay from Hi-Z after ASP_BCLK launching edge | half-cycle mode, load = 50 pF<br>full-cycle mode, load = 150 pF | $t_{DLY:EN}$ | 0<br>10 | 10<br>28 | ns<br>ns |
| | ASP_DOUT load capacitance | ASP_DOUT | — | 0 | 150 | pF |
| Primary Mode, VDD_IO1 = 3.3 V | ASP_FSYNC output sample/frame rate | | Fs | 16 | 384 | kHz |
| | ASP_BCLK frequency | | $f_{BCLK}$ | 2.8224 | 24.576 | MHz |
| | ASP_BCLK duty cycle | | $D_{BCLK}$ | 45 | 55 | % |
| | ASP_FSYNC delay time after ASP_BCLK launching edge | | $t_{D:BCLK–FSYNC}$ | 0 | 20 | ns |
| | ASP_DOUT delay after ASP_BCLK launching edge | half-cycle mode, load = 50 pF<br>full-cycle mode, load = 150 pF | $t_{D:BCLK–DOUT}$ | 0<br>0 | 11<br>13 | ns<br>ns |
| | ASP_DOUT Hi-Z delay after ASP_BCLK latching edge | half-cycle mode, load = 50 pF<br>full-cycle mode, load = 150 pF | $t_{DLY:HiZ}$ | 0<br>0 | 10<br>10 | ns<br>ns |
| | ASP_DOUT delay from Hi-Z after ASP_BCLK launching edge | half-cycle mode, load = 50 pF<br>full-cycle mode, load = 150 pF | $t_{DLY:EN}$ | 0<br>7 | 15<br>28 | ns<br>ns |
| | ASP_DOUT load capacitance | ASP_BCLK<br>ASP_FSYNC<br>ASP_DOUT | — | 0<br>0<br>0 | 50<br>50<br>150 | pF<br>pF<br>pF |
| Secondary Mode, VDD_IO1 = 1.8 V | ASP_FSYNC input sample/frame rate | | Fs | 16 | 384 | kHz |
| | ASP_FSYNC pulse width | | $t_{HI:FSYNC}$ | $1/f_{ASP_BCLK}$ | — | ns |
| | ASP_BCLK frequency | | $f_{BCLK}$ | 1.024 | 24.576 | MHz |
| | ASP_BCLK high period | | $t_{HI:BCLK}$ | 18 | — | ns |
| | ASP_BCLK low period | | $t_{LO:BCLK}$ | 18 | — | ns |
| | ASP_FSYNC setup time before ASP_BCLK latching edge | | $t_{SU:FSYNC}$ | 5 | — | ns |
| | ASP_FSYNC hold time after ASP_BCLK latching edge | | $t_{H:FSYNC}$ | 5 | — | ns |
| | ASP_DOUT delay after ASP_BCLK launching edge | half-cycle mode, load = 50 pF<br>full-cycle mode, load = 150 pF | $t_{D:BCLK–DOUT}$ | 0<br>0 | 15<br>17 | ns<br>ns |
| | ASP_DOUT Hi-Z delay after ASP_BCLK latching edge | half-cycle mode, load = 50 pF<br>full-cycle mode, load = 150 pF | $t_{DLY:HiZ}$ | 0<br>0 | 12<br>12 | ns<br>ns |
| | ASP_DOUT delay from Hi-Z after ASP_BCLK launching edge | half-cycle mode, load = 50 pF<br>full-cycle mode, load = 150 pF | $t_{DLY:EN}$ | 0<br>11 | 15<br>33 | ns<br>ns |
| | ASP_DOUT load capacitance | ASP_DOUT | — | 0 | 150 | pF |


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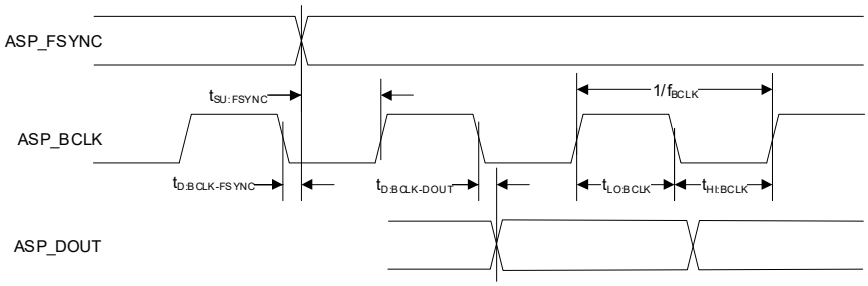
### Table 3-11. Switching Specifications—Audio Serial Port (ASP) *(Cont.)*

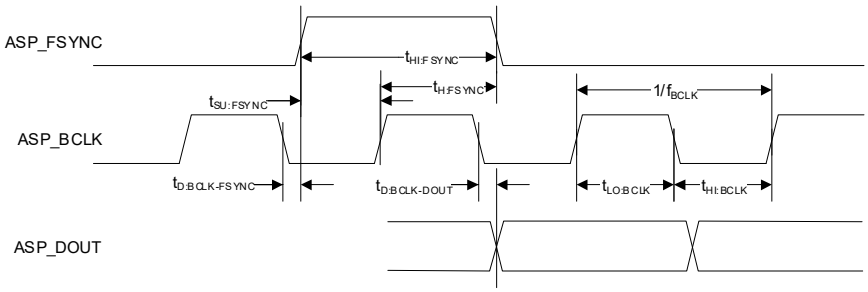
Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO2 = 3.3 V; Ground = GND = GND_A = 0 V; voltages are with respect to ground; input timings are measured at $V_{IL}$ and $V_{IH}$ thresholds, output timings are measured at $V_{OL}$ and $V_{OH}$ thresholds for VDD_IO1 logic (as specified in Table 3-8); $T_A$ = 25 °C.

| Parameter [1,2,3,4,5] | | | Symbol | Minimum | Maximum | Unit |
|---|---|---|---|---|---|---|
| Primary Mode, VDD_IO1 = 1.8 V | ASP_FSYNC output sample/frame rate | | Fs | 16 | 384 | kHz |
| | ASP_BCLK frequency | | $f_{BCLK}$ | 2.8224 | 24.576 | MHz |
| | ASP_BCLK duty cycle | | $D_{BCLK}$ | 45 | 55 | % |
| | ASP_FSYNC delay time after ASP_BCLK launching edge | | $t_{D:BCLK–FSYNC}$ | 0 | 20 | ns |
| | ASP_DOUT delay after ASP_BCLK launching edge | half-cycle mode, load = 50 pF<br>full-cycle mode, load = 150 pF | $t_{D:BCLK–DOUT}$ | 0<br>0 | 16<br>18 | ns<br>ns |
| | ASP_DOUT Hi-Z delay after ASP_BCLK latching edge | half-cycle mode, load = 50 pF<br>full-cycle mode, load = 150 pF | $t_{DLY:HiZ}$ | 0<br>0 | 13<br>13 | ns<br>ns |
| | ASP_DOUT delay from Hi-Z after ASP_BCLK launching edge | half-cycle mode, load = 50 pF<br>full-cycle mode, load = 150 pF | $t_{DLY:EN}$ | 0<br>7 | 15<br>34 | ns<br>ns |
| | ASP_DOUT load capacitance | ASP_BCLK<br>ASP_FSYNC<br>ASP_DOUT | — | 0<br>0<br>0 | 50<br>50<br>150 | pF<br>pF<br>pF |

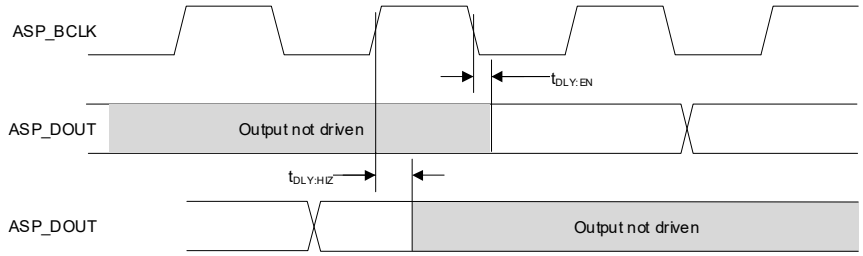
1. The ASP_BCLK launching edge is selectable. Half-cycle mode = ASP_BCLK launching edge is opposite to latching edge. Full-cycle mode = ASP_BCLK launching edge is same as latching edge.
2. ASP timing in I²S and Left-Justified Modes.
   ASP_BCLK can be inverted if required; the figure shows the default polarity.



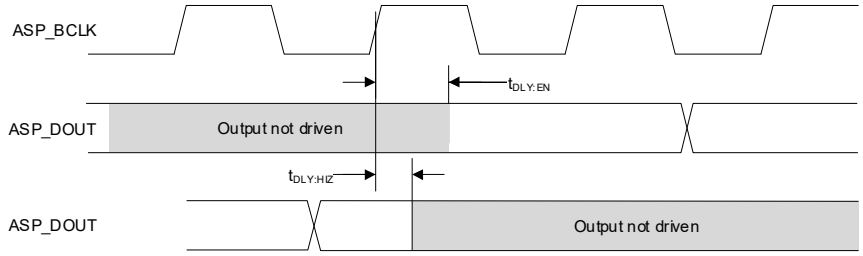

3. ASP timing in TDM Mode.
   ASP_BCLK can be inverted if required; the figure shows the default polarity in half-cycle mode.




4. ASP_DOUT timing for multiple devices sharing the audio serial port bus—half-cycle mode.




5. ASP_DOUT timing for multiple devices sharing the audio serial port bus—full-cycle mode.





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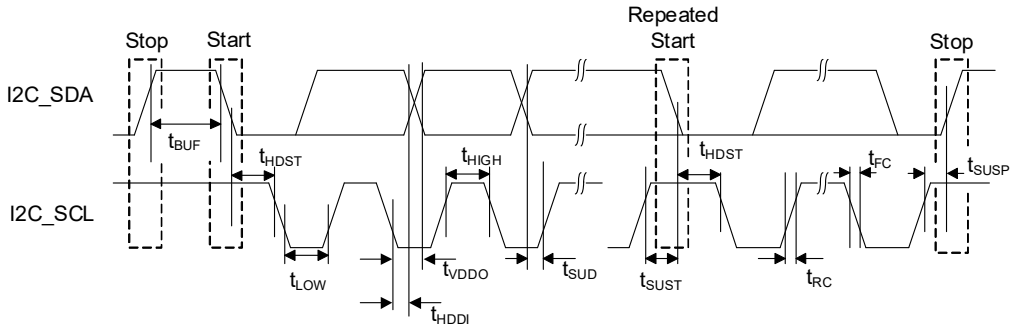
### Table 3-12. Switching Specifications—I²C Control Port

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO1 = VDD_IO2 = 3.3 V; Ground = GND = GND_A = 0 V; voltages are with respect to ground; input timings are measured at $V_{IL}$ and $V_{IH}$ thresholds, output timings are measured at $V_{OL}$ and $V_{OH}$ thresholds for VDD_IO1 logic (as specified in Table 3-8); $T_A$ = 25 °C.

| Parameter [1,2] | Symbol | Minimum | Maximum | Unit |
|---|---|---|---|---|
| SCL clock frequency | $f_{SCL}$ | — | 1000 | kHz |
| Clock low time | $t_{LOW}$ | 500 | — | ns |
| Clock high time | $t_{HIGH}$ | 260 | — | ns |
| Start condition hold time (before first clock pulse) | $t_{HDST}$ | 260 | — | ns |
| Setup time for repeated start | $t_{SUST}$ | 260 | — | ns |
| Rise time of SCL and SDA<br>$f_{SCL}$ ≤ 100 kHz<br>100 kHz < $f_{SCL}$ ≤ 400 kHz<br>400 kHz < $f_{SCL}$ ≤ 1000 kHz | $t_{RC}$ | 600<br>180<br>72 | 1000<br>300<br>120 | ns<br>ns<br>ns |
| Fall time of SCL and SDA<br>$f_{SCL}$ ≤ 100 kHz<br>100 kHz < $f_{SCL}$ ≤ 400 kHz<br>400 kHz < $f_{SCL}$ ≤ 1000 kHz | $t_{FC}$ | 6.5<br>6.5<br>6.5 | 300<br>300<br>120 | ns<br>ns<br>ns |
| Rise time variation between SDA and SCL | — | — | 1.67 | ns |
| Fall time variation between SDA and SCL<br>$f_{SCL}$ ≤ 100 kHz<br>100 kHz < $f_{SCL}$ ≤ 400 kHz<br>400 kHz < $f_{SCL}$ ≤ 1000 kHz | — | —<br>—<br>— | 100<br>100<br>75 | ns<br>ns<br>ns |
| Setup time for stop condition | $t_{SUSP}$ | 260 | — | ns |
| SDA setup time to SCL rising | $t_{SUD}$ | 50 | — | ns |
| SDA input hold time from SCL falling [3] | $t_{HDDI}$ | 0 | — | ns |
| Output data valid (Data/ACK) [4]<br>$f_{SCL}$ ≤ 100 kHz<br>100 kHz < $f_{SCL}$ ≤ 400 kHz<br>400 kHz < $f_{SCL}$ ≤ 1000 kHz | $t_{VDDO}$ | —<br>—<br>— | 3450<br>900<br>450 | ns<br>ns<br>ns |
| Bus free time between transmissions | $t_{BUF}$ | 500 | — | ns |
| SDA bus capacitance | $C_B$ | — | 550 | pF |
| SCL/SDA pull-up resistance | $R_P$ | 500 | — | Ω |
| Pulse width of spikes to be suppressed | $t_{ps}$ | 0 | 50 | ns |

1. All timing is relative to thresholds specified in Table 3-8, $V_{IL}$ and $V_{IH}$ for input signals, and $V_{OL}$ and $V_{OH}$ for output signals.
2. I²C control-port timing.




3. Data must be held long enough to bridge the transition time, $t_{FC}$, of SCL.
4. Time from falling edge of SCL until data output is valid.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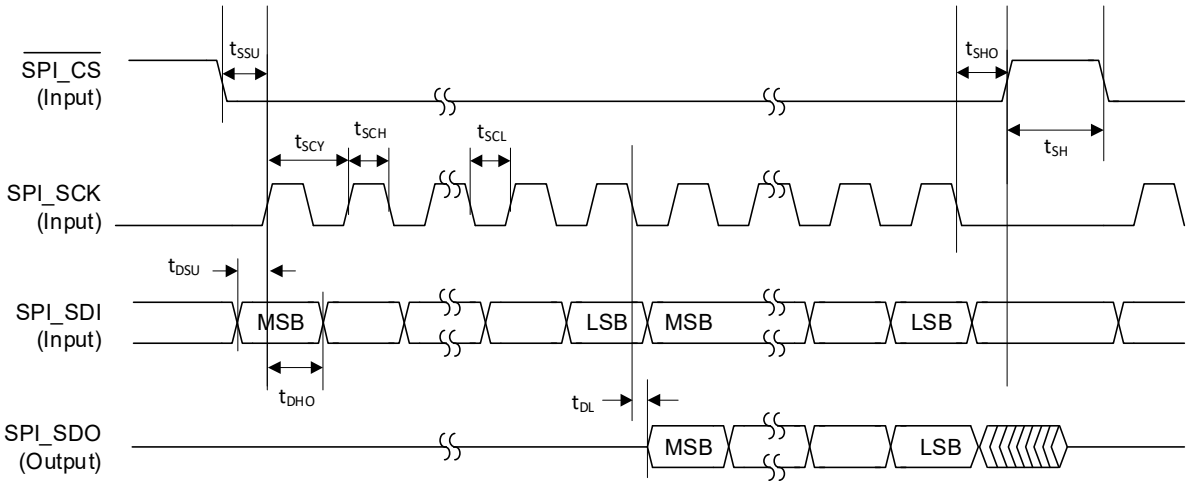
### Table 3-13. Switching Specifications—SPI Control Port

Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO1 = VDD_IO2 = 3.3 V; Ground = GND = GND_A = 0 V; voltages are with respect to ground; input timings are measured at $V_{IL}$ and $V_{IH}$ thresholds, output timings are measured at $V_{OL}$ and $V_{OH}$ thresholds for VDD_IO1 logic (as specified in Table 3-8); $T_A$ = 25 °C.

| Parameter [1] | Symbol | Minimum | Maximum | Unit |
|---|---|---|---|---|
| SPI_SCK frequency | $f_{SCY}$ | — | 24 | MHz |
| $\overline{\text{SPI_CS}}$ falling edge to SPI_SCK rising edge | $t_{SSU}$ | 5 | — | ns |
| SPI_SCK falling edge to $\overline{\text{SPI_CS}}$ rising edge | $t_{SHO}$ | 0.5 | — | ns |
| SPI_SCK pulse width low | $t_{SCL}$ | 18.5 | — | ns |
| SPI_SCK pulse width high | $t_{SCH}$ | 18.5 | — | ns |
| SPI_SDI to SPI_SCK setup time | $t_{DSU}$ | 5 | — | ns |
| SPI_SDI to SPI_SCK hold time | $t_{DHO}$ | 2.5 | — | ns |
| SPI_SCK falling edge to SPI_SDO transition | $t_{DL}$ | 0 | 15 | ns |
| $\overline{\text{SPI_CS}}$ rising edge to SPI_SDO output high-Z | — | 0 | 15 | ns |
| Bus free time between active $\overline{\text{SPI_CS}}$ | $t_{SH}$ | 20 | — | ns |

1.SPI control-port timing.





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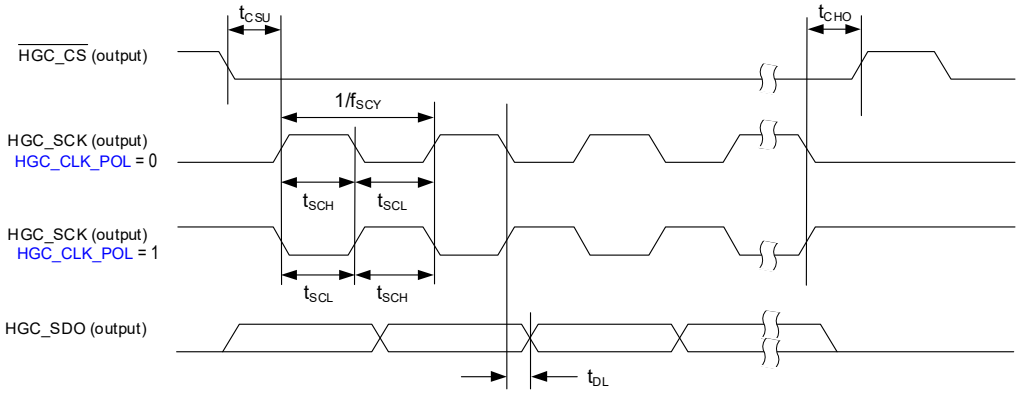
### Table 3-14. Switching Specifications—SPI Controller (Hybrid Gain Control)

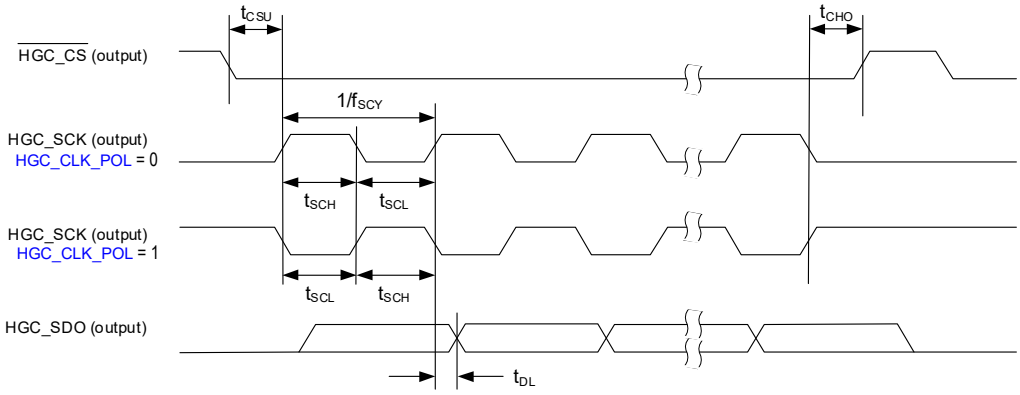
Test conditions (unless specified otherwise in this table): VDD_A = VDD_IO1 = VDD_IO2 = 3.3 V; Ground = GND = GND_A = 0 V; voltages are with respect to ground; output timings are measured at $V_{OL}$ and $V_{OH}$ thresholds for VDD_IO2 logic (as specified in Table 3-8); $T_A$ = 25 °C.

| Parameter [1,2] | | Symbol | Minimum | Maximum | Unit |
|---|---|---|---|---|---|
| HGC_SCK frequency | | $f_{SCY}$ | — | 12.288 | MHz |
| $\overline{\text{HGC_CS}}$ falling edge to HGC_SCK rising edge | | $t_{CSU}$ | 30 | — | ns |
| HGC_SCK falling edge to $\overline{\text{HGC_CS}}$ rising edge | | $t_{CHO}$ | 30 | — | ns |
| HGC_SCK pulse width low | | $t_{SCL}$ | 40 | — | ns |
| HGC_SCK pulse width high | | $t_{SCH}$ | 40 | — | ns |
| HGC_SCK falling edge to HGC_SDO transition | $C_{LOAD}$ (HGC_SDO) = 30 pF<br>$C_{LOAD}$ (HGC_SDO) = 60 pF | $t_{DL}$ | –15<br>–20 | 15<br>20 | ns<br>ns |

1.SPI controller timing, HGC_CLK_PHA = 0.




2.SPI controller timing, HGC_CLK_PHA = 1.





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# 4 Functional Description

## 4.1 Device Power and Reset

The CS5312S is powered using VDD_A1, VDD_A2, VDD_IO1, and VDD_IO2 external supplies.

**Notes:** The VDD_A1 and VDD_A2 rails should be star-connected and powered from a single supply. The associated power domain is referred to as VDD_A.

VDD_IO1 and VDD_IO2 are independent power domains. VDD_IO1 supplies host-related interfaces (e.g., SPI control interface); VDD_IO2 supplies external interfaces (e.g., crystal oscillator connections). Integrated level shifters are included for direct interface to logic levels from 1.8 V to 3.3 V.

There are no power-sequencing requirements—supplies can be enabled in any order.

The CS5312S is in reset if the $\overline{\text{RESET}}$ pin is asserted (Logic 0), or if the VDD_A supply is below the respective reset threshold defined in Table 3-9.

The GND_A pin and the ground paddle, must be tied to a common ground (GND) plane directly underneath the CS5312S.

## 4.2 Hardware Configuration

The CS5312S supports hardware and software control modes. In hardware mode, the device configuration is determined entirely by external resistors connected to the hardware-control pins. In software mode, the I²C/SPI control port is used to configure the device.

In hardware mode, the audio serial port (ASP) configuration is selected using the CONFIG1 and CONFIG2 pins as described in Table 4-1. See Section 4.4 for more details of the sample-rate selection and Section 4.9 for more details of the ASP operation.

**Table 4-1. Hardware Control—ASP Configuration**

| Pin Name | Pin Configuration | | Description |
|---|---|---|---|
| CONFIG1 | Pull-up to VDD_IO1 | 0 Ω | Software control mode (I²C/SPI) |
| | | 4.7 kΩ | In I²C Mode, the pull-up resistor is used to select the device address—see Section 4.10. |
| | | 22 kΩ | In SPI Mode, it is recommended to use a 100 kΩ pull-up resistor. |
| | | 100 kΩ | |
| | Pull-down to GND | 100 kΩ | ASP Primary Mode, 176.4 kHz, 192 kHz sample rate |
| | | 22 kΩ | ASP Primary Mode, 88.2 kHz, 96 kHz sample rate |
| | | 4.7 kΩ | ASP Primary Mode, 44.1 kHz, 48 kHz sample rate |
| | | 0 Ω | ASP Secondary Mode, autodetect sample rate |
| CONFIG2 | Pull-up to VDD_IO1 | 0 Ω | ASP TDM Mode—minimum time slots [1], ASP_FSYNC_TYPE = pulse |
| | | 4.7 kΩ | ASP TDM Mode—maximum time slots [2], data output on BCLK falling edge (half-cycle mode) [3], ASP_FSYNC_TYPE = pulse |
| | | 22 kΩ | ASP TDM Mode—maximum time slots [2], data output on BCLK rising edge (full-cycle mode) [4], ASP_FSYNC_TYPE = pulse |
| | | 100 kΩ | ASP TDM Mode—minimum time slots [1], ASP_FSYNC_TYPE = square wave (50% duty cycle) [5] |
| | Pull-down to GND | 100 kΩ | ASP TDM Mode—maximum time slots [2], data output on BCLK falling edge (half-cycle mode) [3], ASP_FSYNC_TYPE = square wave (50% duty cycle) [5] |
| | | 22 kΩ | ASP TDM Mode—maximum time slots [2], data output on BCLK rising edge (full-cycle mode) [4], ASP_FSYNC_TYPE = square wave (50% duty cycle) [5] |
| | | 4.7 kΩ | ASP Left-Justified Mode |
| | | 0 Ω | ASP I²S Mode |

1. The ASP data format is configured to support two time slots; this is the minimum necessary for the CS5312S output.
2. The ASP data format is configured to support the maximum number of time slots for the applicable BCLK rate, refer to Table 4-15.
3. Half-cycle mode = ASP_DOUT launching edge (BCLK falling) is opposite to the receiving-device latching edge (BCLK rising), refer to Table 3-11.
4. Full-cycle mode = ASP_DOUT launching edge (BCLK rising) is same as the receiving-device latching edge, refer to Table 3-11.
5. ASP_FSYNC_TYPE = square wave (50% duty cycle) is available in ASP Primary Mode only, as described in Section 4.9.


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If the ASP is configured for TDM data format with maximum time slots, the TDM slot selection is determined using the CONFIG3 pin as described in Table 4-2. See Section 4.9 for more details of the ASP TDM modes.

**Table 4-2. Hardware Control—TDM Slot Selection**

| Pin Name | Pin Configuration | | Description |
|---|---|---|---|
| CONFIG3 | Pull-up to VDD_IO1 | 0 Ω | Slots 14–15 [1] |
| | | 4.7 kΩ | Slots 12–13 [1] |
| | | 22 kΩ | Slots 10–11 [1] |
| | | 100 kΩ | Slots 8–9 [1] |
| | Pull-down to GND | 100 kΩ | Slots 6–7 [2] |
| | | 22 kΩ | Slots 4–5 [2] |
| | | 4.7 kΩ | Slots 2–3 |
| | | 0 Ω | Slots 0–1 |

1.Slots 8–15 are only valid in 16-slot TDM Mode.
2.Slots 4–7 are only valid in 8-slot or 16-slot TDM Mode.

The clock-reference and virtual PAD configurations are determined using the CONFIG4 pin as described in Table 4-3. See Section 4.4 for more details of the CS5312S clocking architecture, and Section 4.5.5 for more details of virtual PAD function.

**Table 4-3. Hardware Control—Clocking Configuration**

| Pin Name | Pin Configuration | | Clock Reference | Reference Clock Frequency (MHz)[1] | Virtual PAD |
|---|---|---|---|---|---|
| CONFIG4 | Pull-up to VDD_IO1 | 0 Ω | — | — | Bypassed |
| | | 4.7 kΩ | XTAL | 24.576 or 22.5792 | |
| | | 22 kΩ | — | — | |
| | | 100 kΩ | MCLK | 24.576 or 22.5792 | |
| | Pull-down to GND | 100 kΩ | — | — | Enabled - Level Detection |
| | | 22 kΩ | MCLK | 24.576 or 22.5792 | |
| | | 4.7 kΩ | — | — | Enabled - Edge Detection |
| | | 0 Ω | MCLK | 24.576 or 22.5792 | |

1.The reference clock frequency is related to sample rate options (for supported configurations, see Section 4.4).

In hardware mode, the digital filter is selected using the CONFIG5 pin. See Section 4.8 for more details of the digital filters.

The filter selection is defined in Table 4-4. The filter selection is dependent on the sample rate, as described in Footnote 1 in Table 4-4.

**Table 4-4. Hardware Control—Digital Filter Selection**

| Pin Name | Pin Configuration | | ADC Decimation Filter [1] | High-Pass Filter (HPF) |
|---|---|---|---|---|
| CONFIG5 | Pull-up to VDD_IO1 | 0 Ω | Minimum phase, slow roll-off | Bypassed |
| | | 4.7 kΩ | Minimum phase, fast roll-off | |
| | | 22 kΩ | Linear phase, slow roll-off | |
| | | 100 kΩ | Linear phase, fast roll-off | |
| | Pull-down to GND | 100 kΩ | Linear phase, fast roll-off | Enabled |
| | | 22 kΩ | Linear phase, slow roll-off | |
| | | 4.7 kΩ | Minimum phase, fast roll-off | |
| | | 0 Ω | Minimum phase, slow roll-off | |

1.Fast roll-off filters are supported for all sample rates. Slow roll-off filters are not valid for 16 kHz or 32 kHz sample rates.

In hardware mode, the device configuration is latched when reset is released (either power-on reset or deassertion of the $\overline{\text{RESET}}$ pin). In hardware mode, the configuration cannot be changed while the device is operational. To update the device configuration, the $\overline{\text{RESET}}$ pin must be asserted (Logic 0), or the device power cycled, in order to read new settings on the CONFIGx pins.


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If software mode is selected (i.e., CONFIG1 is pulled-up to VDD_IO1), the device configuration and the digital-filter selection are controlled by register writes via the applicable control interface, as described in Section 4.10. Unused CONFIGx pins should be terminated as described in Section 1.3.

**Note:** In software mode, the CONFIG1 pin is used to select the I²C target address (see Section 4.10). If the SPI control interface is used, it is recommended to connect the CONFIG1 pin to VDD_IO1 via a 100 kΩ resistor.

## 4.3 Software Configuration

Software control mode is enabled if the CONFIG1 pin is pulled-up to VDD_IO1; note that $\overline{\text{RESET}}$ must remain asserted (i.e., Logic 0) until CONFIG_1/$\overline{\text{SPI_CS}}$ is deasserted (i.e., Logic 1). In software control mode, the CS5312S is configured by writing to control registers using the control port.

The control port supports I²C and SPI modes of operation; the applicable mode is detected automatically on the respective interface pins. In I²C mode, the target address is selectable using the CONFIG1 pin. See Section 4.10 for further details of the I²C/SPI control port.

In software control mode, GLOBAL_EN is used as the global control field for enabling/disabling the CS5312S functions. The device should be configured using the applicable control registers before setting GLOBAL_EN.

**Note:** The clocking (Section 4.4) and ASP (Section 4.9) control registers are only valid on the rising edge of GLOBAL_EN. Writing to these registers has no effect at any other time. It is recommended to select the disabled state (GLOBAL_EN = 0) before writing to these registers.

A reset of the CS5312S can be triggered by writing 0x5A to the SW_RESET field. A software reset disables all functions and sets the control registers to their default states.

## 4.4 System Clocking

Clocking for the CS5312S is provided using either the MCLK input or the crystal (XTAL) oscillator. In each case, the frequency is related to sample rate options, as described in Table 4-5:

**Table 4-5. Reference Frequency and Sample Rate Options**

| Reference Source | Reference Frequency (MHz) | Sample Rate (kHz)[1] |
|---|---|---|
| MCLK or XTAL | 22.5792 | 44.1, 88.2, 176.4, 352.8 |
| | 24.576 | 16, 32, 48, 96, 192, 384 |

1. Sample rates 352.8 kHz and 384 kHz are supported in software control mode only (for details of software control mode, see Section 4.4.2).

The specifications for the clocking sources are described in Table 3-10.

In hardware mode, the clock source is configured using the CONFIG4 pin, as detailed in Table 4-3. In software mode, the clocking source is selected using SYSCLK_SRC.

The crystal oscillator uses an external crystal to generate the system clock. Load capacitors are connected to the crystal as shown in Fig. 4-1. A series resistor ($R_S$) may also be required to configure the drive level for the selected crystal.

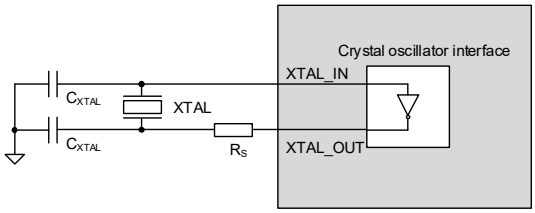


**Figure 4-1. Crystal Oscillator Connection**


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Guidance on selecting a suitable crystal and associated components is provided in Section 5.3.1. The suitability of the external crystal is calculated as a function of the operating voltage (VDD_IO2) and the transconductance of the crystal interface, as defined in Table 3-10.

If clocking is provided using the crystal oscillator, the CS5312S outputs a clock on the MCLK pin. The frequency of the MCLK output clock matches the crystal oscillator frequency. The output clock can be used to drive other devices.

In ASP Secondary Mode, the ASP_FSYNC input is used to control the ADC-sample timing, enabling multiple CS5312S devices to operate synchronously (sample timing is phase aligned) in a system. The external clocks ASP_FSYNC and ASP_BCLK must be derived from a common clock source (i.e., the MCLK input, or the MCLK output when clocking is provided using the crystal oscillator). See Section 4.9 for more details of the ASP.

The clocking architecture is illustrated in Fig. 4-2.

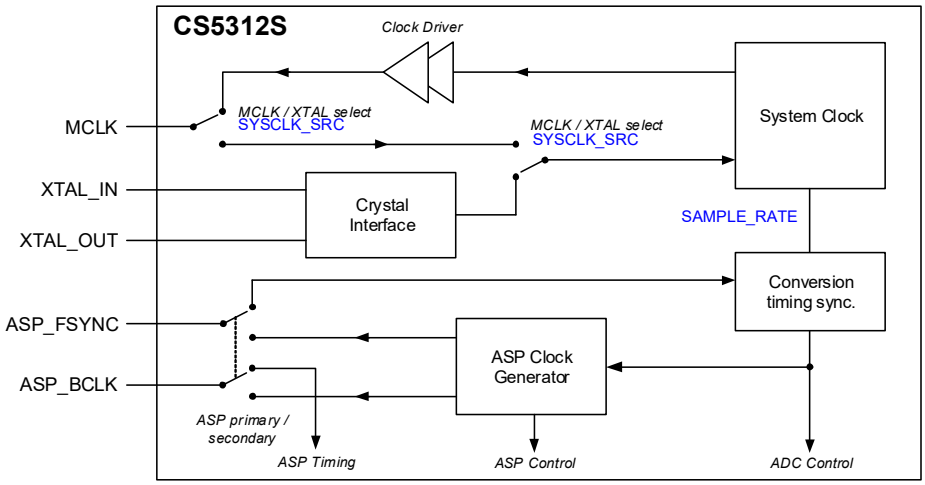


**Figure 4-2. System Clocking**

### 4.4.1 Hardware Control Mode

In hardware control mode, the system clock can be sourced from the MCLK pin or from the crystal oscillator. In each case, the frequency must be:

- 24.576 MHz for sample rates of 16, 32, 48, 96, or 192 kHz
- 22.5792 MHz for sample rates of 44.1, 88.2, or 176.4 kHz

The clock source is configured using the CONFIG4 pin as described in Section 4.2.

The sample rate is selected using the CONFIG1 pin as described in Section 4.2. Sample rates 44.1 kHz–192 kHz can be configured, or else the autodetect option (sample rates 16 kHz–192 kHz) automatically configures the device according to the ASP interface clock signals. The autodetect sample-rate option is only valid if the ASP is operating in Secondary Mode (see Section 4.9).

The supported clocking configurations are summarized in Table 4-6.

**Table 4-6. System Clock Configuration**

| Reference Source | Reference Frequency (MHz) | ASP Operating Conditions [1] |
|---|---|---|
| MCLK or XTAL | 24.576 | Primary or Secondary Mode,<br>I²S, left-justified, or TDM data formats,<br>sample rates 48, 96, and 192 kHz Primary Mode,<br>or sample rates 16, 32, 48, 96, and 192 kHz in Secondary Mode (autodetect only). |
| MCLK or XTAL | 22.5792 | Primary or Secondary Mode,<br>I²S, left-justified, or TDM data formats,<br>sample rates 44.1, 88.2, and 176.4 kHz in Primary Mode,<br>or sample rates 44.1, 88.2, 176.4 kHz in Secondary Mode (autodetect only). |

1. See Section 4.9 for details of the audio serial port (ASP).


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The sample rate must be related to the system clock reference as described in Table 4-7.

**Table 4-7. Hardware Control Mode Sample Rate Options**

| Reference Source | Reference Frequency (MHz) | MCLK Out (MHz) | Sample Rate (kHz) |
|---|---|---|---|
| MCLK | 22.5792 | — | 44.1, 88.2, 176.4 |
| | 24.576 | | 16, 32, 48, 96, 192 |
| XTAL | 22.5792 | 22.5792 | 44.1, 88.2, 176.4 |
| | 24.576 | 24.576 | 16, 32, 48, 96, 192 |

If the ASP is configured in ASP Secondary Mode, the external clocks (MCLK, BCLK, and FSYNC) must be derived from a common clock source and the active BCLK edge must be aligned with the falling MCLK edge. If clocking for the CS5312S is provided using the crystal oscillator, then the BCLK and FSYNC signals should be derived from the common clock source provided by the CS5312S MCLK output, see Section 4.9.

### 4.4.2 Software Control Mode

In software ($I^2C$/SPI) control mode, the clocking configuration is selected using the following control fields:

- The sample rate is configured using SAMPLE_RATE. Sample rates 16 kHz–384 kHz can be configured, or else the autodetect option automatically configures the device according to the ASP interface signals. The sample-rate autodetect option is only valid for sample rates 16 kHz–192 kHz.
- The system clock source is selected using SYSCLK_SRC. The clock source can be either the crystal oscillator or MCLK.
- The system clock frequency must be:
  - 24.576 MHz for sample rates of 16, 32, 48, 96, 192, or 384 kHz
  - 22.5792 MHz for sample rates of 44.1, 88.2, 176.4, or 352.8 kHz

The sample rate must be related to the system clock reference as described in Table 4-8.

**Table 4-8. Software Control Mode Sample Rate Options**

| Reference Source | Reference Frequency (MHz) | MCLK Out (MHz) | Sample Rate (kHz) |
|---|---|---|---|
| MCLK | 22.5792 | — | 44.1, 88.2, 176.4, 352.8 |
| | 24.576 | | 16, 32, 48, 96, 192, 384 |
| XTAL | 22.5792 | 22.5792 | 44.1, 88.2, 176.4, 352.8 |
| | 24.576 | 24.576 | 16, 32, 48, 96, 192, 384 |

The sample-rate autodetect option (16 kHz–192 kHz) is only valid if the ASP is operating in Secondary Mode (see Section 4.9).

If the ASP is configured in ASP Secondary Mode, the external clocks (MCLK, BCLK, and FSYNC) must be derived from a common clock source and the active BCLK edge must be aligned with the falling MCLK edge. If clocking for the CS5312S is provided using the crystal oscillator, then the BCLK and FSYNC signals should be derived from the common clock source provided by the CS5312S MCLK output, see Section 4.9.

## 4.5 ADC and Analog Input

The CS5312S supports two analog input channels, each incorporating a high-performance sigma-delta analog-to-digital converter (ADC) with integrated programmable analog gain. Digital volume and mute control is also provided on each input channel.

The analog gain, digital volume, and mute controls are supported in software ($I^2C$/SPI) control mode only.


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### 4.5.1 ADC Path Enable

The analog input and ADC paths are enabled using INx_ADC_EN (where x indicates the channel number 1–2).

**Note:** Both input paths (1–2) must always be configured in the same state (enabled or disabled). For example, input path 1 should not be enabled without also enabling input path 2.

The polarity of the ADC output can be inverted using INx_INV for the respective channel.

### 4.5.2 ADC Digital Volume and Mute

The ADC signal path incorporates a digital volume control, supporting a range of –127.5 dB to +30 dB in 0.5 dB steps. Volume ramping and digital mute is also supported.

The digital volume is configured using INx_VOL for the respective input channel. The digital mute is enabled by setting INx_MUTE.

Writing to the volume or mute fields has no effect on the signal path until a 1 is written to IN_VU. Writing 1 to IN_VU causes the volume and mute settings to be updated on all input paths simultaneously.

When the volume or mute is changed, the digital gain of the affected signal paths is ramped up or down to the new setting. For increasing gain, the rate is controlled by IN_RAMP_RATE_INC; for decreasing gain, the rate is controlled by IN_RAMP_RATE_DEC.

**Note:** The IN_RAMP_RATE_INC and IN_RAMP_RATE_DEC fields should not be changed while a volume ramp is in progress.

### 4.5.3 Input Path Analog and Digital Gain

The ADC signal path incorporates analog gain, minimizing external component requirements. The analog gain enhances overall system efficiency and performance by delivering superior input-referred noise and maintaining signal integrity between different applications.

The analog gain is configurable to 0 dB, 6 dB, or 12 dB. The maximum differential input signal level at each gain setting is shown in Table 4-9.

**Table 4-9. Maximum Input Signal Level per Internal Analog Gain Setting**

| Internal Analog Gain (dB) | Maximum Input Signal Level ($V_{RMS}$) |
|---|---|
| 0 | 2 |
| 6 | 1 |
| 12 | 0.5 |

The ADC path incorporates digital gain, supporting a range of –32 dB to +31.875 dB in 0.125 dB steps. The digital gain provides fine adjustment of the overall input path gain, optimizing the dynamic range of the signal path across a wide range of signal levels.

#### 4.5.3.1 Gain Control

Zero-cross detection is used to synchronize the analog and digital gain changes, avoiding audible gain-change transients.

The analog gain is configured for each channel using the respective INx_INT_ANA_GAIN bit (where x indicates the channel number 1–2). If enabled, both channels are configured with 0 dB gain by default.

The digital gain is configured for each channel using INx_INT_DIG_GAIN. Gain ramping is also supported (as described in Section 4.7).

The gain changes are applied upon register write using INx_UPDATE.

**Note:** The digital volume and digital gain are configured separately. The total digital gain of the input path is the sum of the digital volume and digital gain. Digital volume is described in Section 4.5.2.


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### 4.5.4 Input Clip Warning

The CS5312S provides a clip-warning function on the ADC input paths; this can be used to provide a warning of large or clipped signal levels.

The clip-warning threshold level is configured using IN_CLIP_THRESH. The selected level applies to both input channels.

Clip warning provides input to the interrupt controller (see Section 4.11). If an input signal exceeds the clip-warning threshold, the INx_CLIP_WARN_INT bit is set (where *x* indicates the channel number 1–2). These bits are latching fields which, once set, remain set until a 1 is written to the respective bits; these bits can be polled at any time or in response to the IRQ output signal being asserted.

### 4.5.5 Virtual PAD

The CS5312S includes a virtual PAD function that emulates a conventional PAD with minimal impact on the noise floor; this reduces external component requirements, leading to a more compact and efficient design.

If virtual PAD is used, an external preamplifier attenuates the input signal, emulating a PAD-on status. To emulate a PAD-off status, corresponding gain is applied to compensate for the external attenuation. This architecture ensures a consistent anti-aliasing filter response in either state.

A logic input to a GPIO pin can be used to select PAD-on/off status. In software mode, the PAD-on/off status can also be selected by writing to control registers via the applicable control interface.

If a logic input to a GPIO pin is used to select PAD-on/off status, edge or level detection is supported.

- If edge detection is selected, a rising-edge input on a GPIO pin toggles the PAD-on/off status for each channel. The PAD-on/off status for each channel is provided as a logic output on a GPIO pin; this can be used, for example, to control LEDs for visual indication. The Logic 1 output indicates the PAD-off status; the Logic 0 output indicates the PAD_on status.
- If level detection is selected, a Logic 1 input on a GPIO pin selects PAD-off status and a Logic 0 input selects PAD-on status; a logic output is not provided. The logic levels are described in Table 3-8.

**Note:** The GPIO logic levels are referenced to the VDD_IO2 domain; level shifting may be required if connecting to a host interface operating at a different level (see Table 3-8 for details).

Virtual PAD is supported in hardware and software modes.

#### 4.5.5.1 Hardware Mode

In hardware mode, the virtual PAD function supports a fixed external attenuation of 20 dB. The CS5312S analog and digital gains are configured to provide +20 dB gain if PAD-off status is selected and 0 dB gain if PAD-on status is selected.

**Note:** Virtual PAD is only supported in hardware mode if the system clock is sourced from MCLK.

Edge or level detection is configured using the CONFIG 4 pin, as shown in Table 4-3.

If edge detection is selected, the GPIO pins as assigned as described in Table 4-10.

**Table 4-10. Virtual PAD Edge Detection GPIO Configuration**

| Pin Number | Pin Name | Function |
|---|---|---|
| 14 | GPIO1 | Channel 1 output |
| 15 | GPIO2 | Channel 2 output |
| 17 | GPIO3 | Channel 1 input |
| 18 | GPIO4 | Channel 2 input |


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If level detection is selected, the GPIO pins are assigned as described in Table 4-11.

**Table 4-11. Virtual PAD Level Detection GPIO Configuration**

| Pin Number | Pin Name | Function |
|---|---|---|
| 14 | GPIO1 | — |
| 15 | GPIO2 | — |
| 17 | GPIO3 | Channel 1 input |
| 18 | GPIO4 | Channel 2 input |

#### 4.5.5.2 Software Mode

In software mode, the virtual PAD function supports a configurable external preamplifier gain; for PAD-on, a maximum attenuation of 20 dB is supported. HGC synchronizes adjustments across the combined external and internal gain range (HGC operation is described in Section 4.7).

- To emulate PAD-off status, the external analog gain is configured for each channel using INx_HIGH_EXT_ANA_GAIN, and the internal analog and digital gains are configured for each channel using INx_HIGH_INT_ANA_GAIN and INx_HIGH_INT_DIG_GAIN respectively (where *x* indicates the channel number 1–2).
- To emulate PAD-on status, the external analog gain is configured for each channel using INx_LOW_EXT_ANA_GAIN, and the internal analog and digital gains are configured using INx_LOW_INT_ANA_GAIN and INx_LOW_INT_DIG_GAIN respectively.

The external analog gain can be controlled using the HGC SPI control interface or by logic level output on GPIO pins; HGC SPI or GPIO control is selected using HGC_CTRL_INTERFACE. If the HGC SPI control interface is selected, GPIO functions are not supported on the $\overline{\text{HGC_CS}}$/GPIO2, XTAL_IN/HGC_SDO/GPIO3, and XTAL_OUT/HGC_SCK/GPIO4 pins,

If the HGC SPI control interface is selected, the bit patterns corresponding to the external gain selections are configured for each channel using the respective INx_HIGH_BIT_PATT and INx_LOW_BIT_PATT fields. If GPIO control is selected, the GPIO1–4 pin output levels are configured using bits 12–15 respectively of INx_HIGH_BIT_PATT_1 and INx_LOW_BIT_PATT_1.

**Note:** The INx_HIGH_BIT_PATT and INx_LOW_BIT_PATT bit patterns are a maximum of 32 bits. The bit pattern length is configured for each channel using INx_BIT_PATT_LENGTH, the selected length applies to both bit patterns. If the bit pattern is 16 bits or less, it is stored in the INx_HIGH_BIT_PATT_1 and INx_LOW_BIT_PATT_1 fields. The MSB represents the first-transmitted bit of the pattern; one or more of the LSBs may be unused, depending on the size of the bit pattern. If the bit pattern is more than 16 bits, the remaining bits are stored in INx_HIGH_BIT_PATT_0 and INx_LOW_BIT_PATT_0.

The internal and external gain configuration settings do not take effect until the PAD-on/off status is selected. PAD-off status can be selected by writing 1 to INx_HIGH_UPDATE; PAD-on status can be selected by writing 1 to INx_LOW_UPDATE.

PAD-on/off selection provides input to the interrupt controller, described in Section 4.11. If INx_HIGH_UPDATE and INx_LOW_UPDATE are set concurrently (i.e., PAD-on status and PAD-off status are both selected simultaneously), an interrupt event is indicated using GAIN_CONFLICT_INT. This is a latching bit which, once set, remains set until a 1 is written. This bit can be polled at any time or in response to the IRQ output signal being asserted.

The PAD-on/off status can be selected by a logic input to a GPIO pin; the pin is selected using the respective INx_GPI_SEL bits. Edge or level detection (described in Section 4.5.5) is configured using SW_TYPE; the debounce time is configurable using DB_TIME.

- If edge detection is selected, the input polarity can be inverted for each channel using the respective INx_GPI_POL bits.
- If level detection is selected, a Logic 1 input selects PAD-off status and a Logic 0 input selects PAD-on status.


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The PAD-on/off status for each channel can be configured as a logic output on a GPIO pin; the pin is selected using the respective INx_GPO1_SEL to INx_GPO4_SEL bits. For PAD-on status, the output logic levels for pins GPIO1–4 are configured using bits 12–15 respectively of INx_LOW_BIT_PATT_1; for PAD off status, the output logic levels for pins GPIO1–4 are configured using bits 12–15 respectively of INx_HIGH_BIT_PATT_1. Note that if one or more GPIO pins are used to control external gain, the same GPIO pins cannot be used for virtual PAD functions.

**Notes:** Pins GPIO3 and GPIO4 are not available if the system clock is sourced from the crystal oscillator.

The GPIO logic levels are referenced to the VDD_IO2 domain; level shifting may be required if connecting to a host interface operating at a different level (see Table 3-8 for details).

The current status for each GPIO pin is indicated using GPI_STS and GPO_STS. If the input polarity is inverted (i.e., the INx_GPI_POL bits are set), the GPI_STS bits indicate the opposite logic level to the GPIO pin status.

#### 4.5.5.3 Automatic PAD Response

In software mode, the virtual PAD function incorporates a level detector on the ADC input channels to selectively determine whether the PAD should be turned on. This can be used to prevent clipping of large signals at the ASP output without requiring host intervention. The level detector is enabled on each audio channel using the respective INx_PAD_LD_EN bit (where x indicates the channel number 1–2).

Signal detection for the high-level threshold uses either the instantaneous or averaged signal level; this is selected using IN_PAD_LD_AVG. Signal detection for the low-level threshold uses the averaged signal level. The averaged signal level is calculated using an exponential moving average (EMA) function; the time constant is configurable using IN_PAD_LD_TIME.

The high and low thresholds associated with the virtual PAD level detector are configured using INx_PAD_HIGH_THR and INx_PAD_LOW_THR respectively.

**Note:** Thresholds described in INx_PAD_HIGH_THR are for signal detection using the averaged signal level; if the instantaneous signal level is selected, the thresholds are approximately 4 dB lower than stated.

If the input signal exceeds the high-level threshold, the CS5312S can automatically select PAD-on status. Automatic PAD response is enabled using INx_PAD_AUTO_EN. Note that PAD-on status remains selected until PAD-off is selected by a Logic 1 input to a GPIO pin or by writing 1 to INx_HIGH_UPDATE.

Automatic PAD response provides input to the interrupt controller, described in Section 4.11. If the input signal exceeds the low-level threshold, the INx_PAD_LOW_INT bit is set. If the input signal exceeds the high-level threshold, the INx_PAD_HIGH_INT bit is set. These bits are latching fields which, once set, remains set until a 1 is written. These bits can be polled at any time or in response to the IRQ output signal being asserted; the host can use these bits to determine whether to turn the PAD-on, or to turn the PAD-off (including after an automatic response).

## 4.6 Signal-Activity Detection

The CS5312S incorporates a signal-activity detection function on the ADC input paths. Signal-activity detection controls the logic level condition of the CH_IDLE output pin—the Logic 0 condition indicates signal activity on one or more input; the Logic 1 condition indicates no signal activity on all inputs.

The CH_IDLE pin is an open-drain output, allowing multiple devices to drive the Logic 0 condition in a wired-OR configuration. In a typical application, the host monitors the CH_IDLE logic level condition to determine the input signal-activity status. An external pull-up resistor, typically 10 kΩ, is required on the CH_IDLE pin.

Signal activity is detected on enabled ADC input channels; controls such as volume and mute have no effect on signal-activity detection. If any input channels are disabled using INx_ADC_EN, signal activity on the disabled path(s) does not contribute to the logic-level condition of the CH_IDLE output pin.

Signal-activity detection is enabled on the ADC input paths by writing 0x3 to IN_SIG_ACT_EN.


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If signal-activity detection is enabled on the ADC input paths, the signal level on each channel is monitored against configurable high- and low-level thresholds. The high-level threshold for each channel is configured using the respective INx_SIG_ACT_HIGH_THR bits (where x indicates the channel number 1–2); the low-level threshold for each channel is configured using INx_SIG_ACT_LOW_THR. If signal-activity detection is enabled on the ADC paths, the CH_IDLE behavior is:

- If the signal level on any input channel exceeds the high-level threshold, CH_IDLE is driven low (Logic 0).
- If the signal level on all input channels falls below the low-level threshold, CH_IDLE is pulled high (Logic 1).

Signal-activity detection uses an averaged signal level that is calculated using an exponential moving average (EMA) function. The EMA function for each ADC input channel is enabled using INx_EMA_EN respectively. Note that the input path EMA function is also associated with the transient mask function, described in Section 4.7.The time constant is selected using IN_EMA_TIME.

If signal-activity detection is enabled on the ADC input paths and the EMA function for any input channel is disabled, signal activity on that channel will not be detected—CH_IDLE will not be driven low (Logic 0) by signal activity on that channel. It is recommended to enable the EMA function for all input channels.

## 4.7 Hybrid Gain Control

The CS5312S provides the capability to control an external gain stage associated with the ADC input path. In typical applications, a separate gain control manages the external gain changes. The hybrid gain control (HGC) function enables synchronized adjustments across the combined external and internal gain range; this enables fine-resolution gain changes without audible artifacts due to external gain step changes.

A configurable transient-masking function is integrated with the gain-control circuits; this enables seamless gain adjustment by actively suppressing the switching transients often associated with the input analog gain selection.

The external analog gain can be controlled by the CS5312S using the HGC SPI control interface implemented on the HGC_CS, HGC_SCK, and HGC_SDO pins, as illustrated in Fig. 4-3. The HGC SPI control interface is not available if the system clock is supplied using the crystal oscillator.

**Note:** If the HGC SPI control interface is selected, GPIO functions are not supported on the GPIO2, GPIO3, GPIO4 pins.

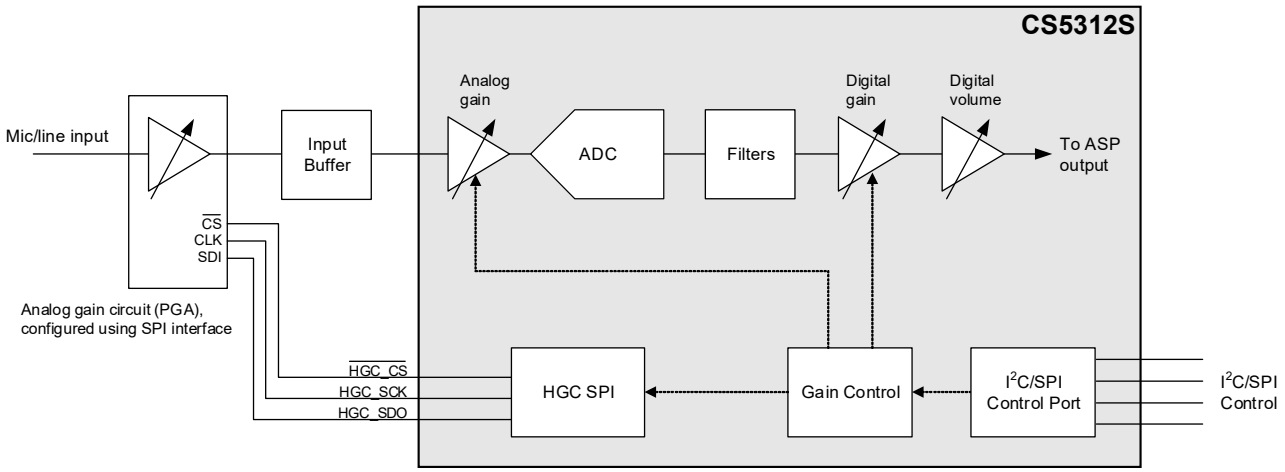


**Figure 4-3. Hybrid Gain Control using HGC SPI**


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Alternatively, the GPIO pins can be configured to control the external analog gain; an example using GPIO1 and GPIO2 is shown in Fig. 4-4. The control type, SPI or GPIO (default), is selected using HGC_CTRL_INTERFACE.

**Note:** GPIO3 and GPIO4 are not available if the system clock is supplied using the crystal oscillator.

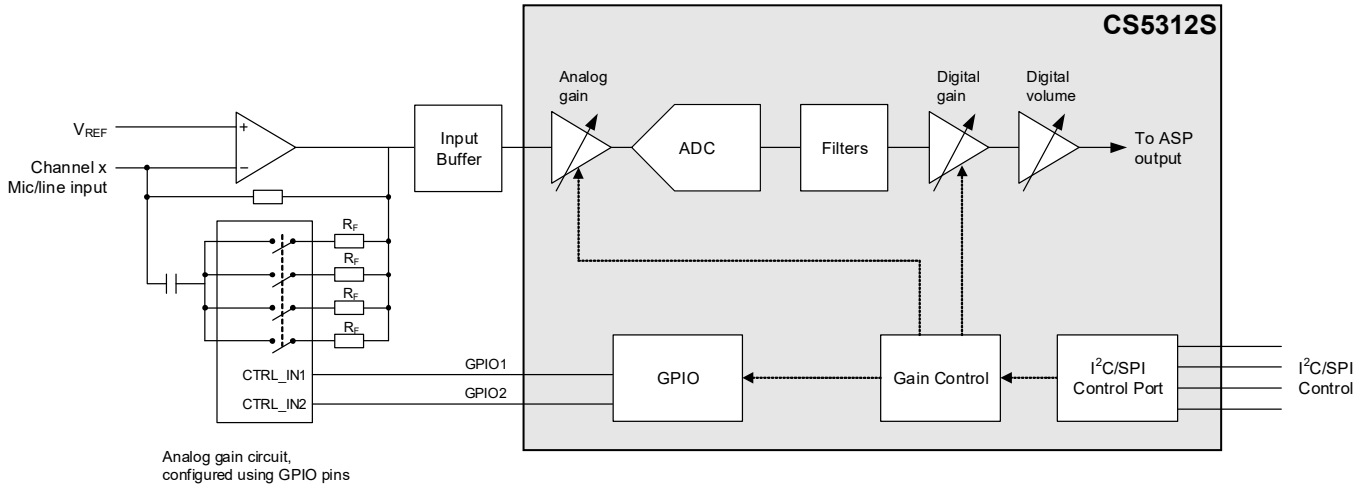


**Figure 4-4. Hybrid Gain Control using GPIO Pin**

To configure the signal path, the host processor writes gain control data to the CS5312S. If the HGC SPI interface has been selected, the CS5312S forwards the data to the external analog gain stage; if the GPIOs have been selected, the CS5312S configures the required GPIO output logic levels. If HGC SPI control is used, multiple external analog gain stages can be independently controlled in a configurable daisy-chain arrangement, as described in Section 4.7.1.

Zero-cross detection is used to synchronize the external gain configuration with the input signal and with the internal gain configurations ensuring seamless operation across the combined gain range.

Volume ramping is supported on the digital volume (see Section 4.5.2); the volume ramp is coordinated with the internal and external gain controls, enabling smooth transitions across the full range of the internal and external gain selections.

**Note:** The digital volume and digital gain are configured separately. The total digital gain of the output path is the sum of the digital volume and digital gain.

The HGC SPI controller interface can also be used to control auxiliary functions associated with the input path using a port expander or similar external IC.

### 4.7.1 HGC SPI Controller Interface Configuration

The HGC SPI controller interface is supported using the $\overline{\text{HGC_CS}}$/GPIO2, XTAL_IN/HGC_SDO/GPIO3, and XTAL_OUT/HGC_SCK/GPIO4 pins, which must be configured for the SPI function if required. The HGC SPI function is selected using HGC_CTRL_INTERFACE. The interface comprises three connections as follows:

- HGC_SCK = Clock output
- HGC_SDO = Data output
- $\overline{\text{HGC_CS}}$ = Chip select ($\overline{\text{CS}}$), active low

**Note:** The HGC SPI interface connections are powered by VDD_IO2; see Table 3-8 for digital I/O levels.

The CS5312S configures the external analog gain circuits using a bit pattern that is transmitted to each of the connected devices in a daisy-chain manner. The bit pattern is shifted through each of the connected devices according to a configurable position in the chain, allowing each device to be individually controlled via a shared data interface.

The HGC SPI interface is fully configurable and flexible to support a wide variety of external gain-control implementations. The HGC SPI data definition is not fixed on the CS5312S; the HGC SPI data can be configured to support whatever bit patterns are required in the specific application.


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A maximum of four devices can be controlled, including two auxiliary devices, as described in Section 4.7.6. The number of bits associated with each connected device is configured for the respective audio channel using INx_BIT_PATT_LENGTH and for the auxiliary devices using AUXx_BIT_PATT_LENGTH.

Each connected device is allocated a position in the daisy chain using the respective INx_SPI_POSITION and AUXx_SPI_POSITION bits. The devices must be assigned to consecutive positions, starting with position 000. The daisy-chain wiring of the external devices must be in the same order as the allocated positions; this ensure each device is configured with its corresponding bit pattern.

The bit pattern length and device position bits should be set to 0 for any audio channel where there is no associated device to be controlled.

If the bit pattern or the device position bits are updated, the new settings are latched internally and are not reflected in the HGC SPI data output until a 1 is written to HGC_INIT_UPDATE. The host processor must confirm that the gain controller is idle (HGC_BUSY_STS = 0) before writing to HGC_INIT_UPDATE.

Example connections are shown in Fig. 4-5.

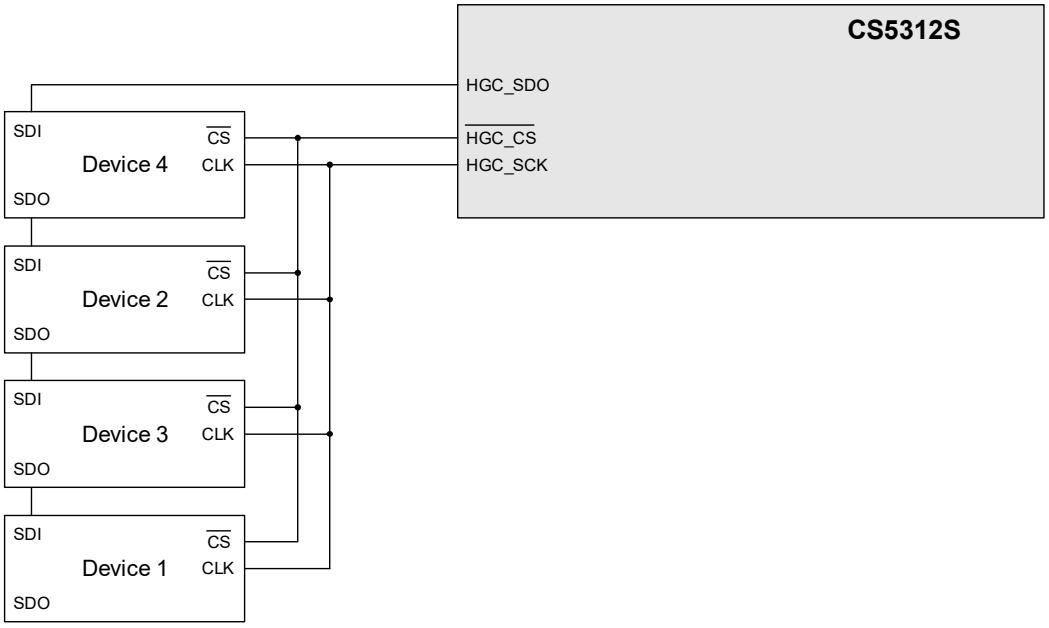


**Figure 4-5. HGC SPI Daisy Chain Example Connections**

In this example, Device 1 and Device 3 are connected to input/ channels 1 and 2 respectively and there are two auxiliary devices, Device 2 and Device 4. The order that the devices are to be serviced in, i.e., the order that they are connect in the daisy chain is Device 1, Device 3, Device 2, and Device 4 Table 4-12.

**Table 4-12. Example SPI Position Configuration**

| Device | Position | Configuration |
|---|---|---|
| Device 1 | 1 | IN1_SPI_POSITION = 000 |
| Device 2 | 3 | AUX1_SPI_POSITION = 010 |
| Device 3 | 2 | IN2_SPI_POSITION = 001 |
| Device 4 | 4 | AUX2_SPI_POSITION = 011 |

The HGC SPI controller is configurable to support different timing and signal-polarity options. The HGC_CLK_POL bit controls the polarity of the clock output; the HGC_CLK_PHA bit controls which phase of the clock cycle the data output is valid. See Table 3-14 for timing specifications.

The HGC SPI clock rate is derived as an integer division of the system clock.

- For 48 kHz-related sample rates, the HGC SPI clock is an integer division of the 24.576 MHz system clock
- For 44.1 kHz-related sample rates, the HGC SPI clock is an integer division of the 22.5792 MHz system clock.


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The HGC SPI clock rate is configured using HGC_SCK_DIV; the fastest HGC SPI clock is 12.288 MHz for 48 kHz-related sample rates, or 11.2896 MHz for 44.1 kHz related sample rates. Slower clock rates can be used to ensure correct timing of the bus signals in applications where a large load capacitance is connected to the HGC SPI outputs.

The minimum idle period between HGC SPI transactions is configured using HGC_CSB_IDLE_DUR. The delay between the falling $\overline{CS}$ edge and the first SCK edge is configured using HGC_CSB_FALL_DLY. The minimum delay between the last SCK edge and the rising $\overline{CS}$ edge is configured using HGC_CSB_RISE_DLY.

In normal operation, the timing of the rising $\overline{CS}$ edge is controlled automatically by the zero-cross detection; the HGC_CSB_RISE_DLY field determines the minimum delay.

### 4.7.2 GPIO Configuration

External gain control using GPIO output is supported using pins GPIO1, HGC_CS/GPIO2, XTAL_IN/HGC_SDO/GPIO3, and XTAL_OUT/HGC_SCK/GPIO4, which must be configured for GPIO use if required. External gain configuration using the GPIO output is selected using HGC_CTRL_INTERFACE.

The GPIO pins are configured as outputs using INx_GPO1_SEL to INx_GPO4_SEL (where x indicates the channel number 1–2). Pins GPIO3 and GPIO4 are not available if the system clock is supplied by the crystal oscillator.

The GPIO pins are powered by VDD_IO2; see Table 3-8 for digital I/O levels.

### 4.7.3 Gain Control Optimization

The CS5312S provides tunable parameters to minimize any audible artifacts when changing the gain configuration. After configuring the external gain, by clocking out the HGC SPI bit pattern or configuring the required GPIO control fields, the CS5312S waits for a zero-cross point in the affected audio channel before completing the HGC SPI transaction (by deasserting the $\overline{CS}$ signal) or updating the GPIO output logic levels. This ensures the gain change is aligned with a zero-cross point on the input signal, on the assumption that deasserting the $\overline{CS}$ (Logic 1) or configuring the GPIO output logic levels causes the new gain setting to be applied immediately in the external circuit. A timeout for zero-cross detection is configured using IN_ZC_TIMEOUT.

After the external gain is updated, the CS5312S waits for a configurable delay before completing the internal analog gain change. The delay is used to align the internal analog gain update with the external analog gain update in the audio stream. The internal analog delay is configured using IN_INT_ANA_GAIN_DLY; this field should be set to equal the total external input path delay (i.e., external input analog gain circuit + input buffer) even if no internal analog gain change is required. The delay should be rounded down for the purposes of selecting the nearest IN_INT_ANA_GAIN_DLY option.

To align the digital gain update with the internal analog gain update in the audio stream, the CS5312S waits for a configurable digital gain delay before completing the internal digital gain counter step and ramp change. The digital counter step is equal to the sum of the external and internal analog gain steps. The digital gain delay is configured using IN_INT_DIG_GAIN_DLY; this field should be set equal to the ADC filter group delay. The ADC filter characteristics are specified in Table 3-5. The delay should be rounded down for the purposes of selecting the nearest IN_INT_DIG_GAIN_DLY option.

A transient-masking function is available on the input path; this is enabled using IN_TM_EN. If enabled, the CS5312S repeats one audio sample for the duration of the transient period, masking the artifact arising from the gain change.

The IN_TM_DLY field defines the time from the external analog gain update to the onset of the transient masking. For typical use cases, the IN_TM_DLY field should be less than or equal to the IN_INT_DIG_GAIN_DLY. The duration of the transient period masking is configured using IN_TM_HOLD_TIME.

Transient masking is most effective on low-amplitude signals and is not recommended for larger signals. The CS5312S incorporates a level detector to selectively determine whether the masking should be applied. The threshold for transient masking is configured using the respective INx_TM_LD_THR bit (where x indicates the channel number 1–2); masking is applied if the signal level is below the threshold.

The level detector uses an averaged signal level that is calculated using an exponential moving average (EMA) function. The EMA function is enabled on each input path using the respective INx_EMA_EN bit. The time constant is selected using IN_EMA_TIME. If the EMA function is disabled, transient masking is applied regardless of the signal level. Note that the transient masking EMA function is also associated with the signal-activity detection function, for further information see Section 4.6.


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### 4.7.4 Audio Channel Gain Control

The host processor configures the external analog, internal analog, and internal digital gain for each audio channel by writing to the respective INx_EXT_ANA_GAIN, INx_INT_ANA_GAIN, and INx_INT_DIG_GAIN fields.

The host must also write the INx_BIT_PATT fields to provide the bit pattern to configure the external device for the required analog gain. If the GPIOs are used, the GPIO output logic levels are determined by bits 12–15 of the INx_BIT_PATT_1 fields.

**Note:** The INx_BIT_PATT bit pattern is a maximum of 32 bits (the size is configured using INx_BIT_PATT_LENGTH). If the bit pattern is 16 bits or less, it is stored in the INx_BIT_PATT_1 field. The MSB represents the first-transmitted bit of the pattern; one or more of the LSBs may be unused, depending on the size of the bit pattern. If the bit pattern is more than 16 bits, the remaining bits are stored in INx_BIT_PATT_0.

The analog and digital gain settings do not become effective immediately on updating the control fields. Writing 1 to INx_UPDATE initiates the update for the respective audio channel and queues the update to be applied; the CS5312S services each updated channel in turn and applies the respective gain settings at the earliest opportunity, dependent on the zero-cross detection for each affected channel.

The HGC_BUSY_STS bit, if set, indicates that gain updates are pending for one or more audio channels (i.e., gain settings have been written to the CS5312S, but not yet applied to the respective audio paths). The bit is cleared automatically when all updates have been applied to the respective channels.

The gain settings, including external gain bit patterns or GPIO output level settings, for each audio channel can be written at any time, regardless of whether an earlier update is currently pending for that channel.

If an audio channel is enabled, but does not have any associated HGC SPI or GPIO-controlled external gain circuit, the external and internal analog gain and digital gain for the respective channel must be maintained at 0 dB (default).

For efficiency of the host-processor interactions, the input path path bit pattern and gain fields can be written as a contiguous block (i.e., one auto-incrementing I²C/SPI write operation). The INx_UPDATE bits can be set in the same I²C/SPI operation as writing to the corresponding INx_INT_DIG_GAIN bits.

**Note:** If the INx_UPDATE bits are written 0 when updating the gains or bit-pattern fields, the settings are latched internally but the updates are not applied to the audio path and do not cause the HGC_BUSY_STS bit to be set. Writing 0 to INx_UPDATE is used in the initialization steps described in Section 4.7.7. Prior to writing 1 to any of the INx_UPDATE bits, HGC must be initialized as described in Section 4.7.7.

### 4.7.5 Gain Ramping Control

The CS5312S supports independent control of the external analog, internal analog, and digital gain stages of the input path. When the digital gain is updated, the gain is ramped up or down to the new value. When the external and internal analog gains are updated, the CS5312S uses digital control to provide a ramped response, masking the larger step size of the analog gain.

For example, if the external analog gain is increased by 3 dB, the gain step is initially canceled out by decreasing the digital gain by 3 dB. Following this, the digital gain is smoothly ramped up by 3 dB to give the desired overall gain.

Gain ramping is supported for changes in analog gain up to a maximum step size of ±32 dB. The digital adjustment used to cancel the initial analog step is supported using a combination of the digital gain and digital volume functions.

Note there is no restriction on whether the external and internal gains are updated in the same operation—the gain ramping is supported for all combinations.


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The gain ramping is illustrated in Fig. 4-6.

In Fig. 4-6, the initial overall gain is 2 dB and a gain of 4 dB is required. The total external plus internal analog gain is updated by +3 dB from 0 dB to 3 dB. The digital gain is initially set to –1 dB, providing the –3 dB counter step to the analog gain step, and then ramped to +1 dB. This gives a smooth transition from 2 dB to 4 dB in the overall (analog + digital) response.

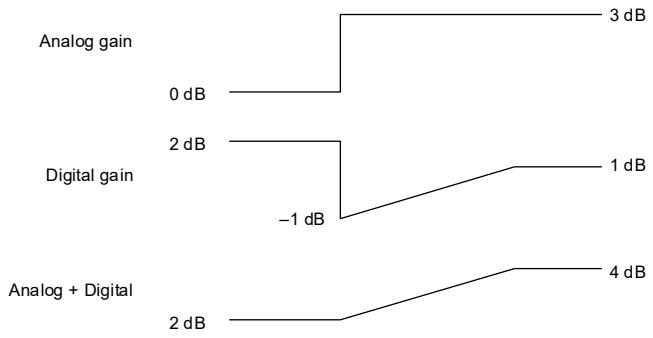


**Figure 4-6. Gain Ramping**

The digital gain counter step and ramp response is configured using IN_STEP_RAMP_EN. If this bit is set, the CS5312S applies the digital gain counter step to mask the analog gain steps. If this bit is clear, there is no masking of the analog gain steps.

For increasing gain, the ramp rate is controlled by IN_RAMP_RATE_INC; for decreasing gain, the rate is controlled by IN_RAMP_RATE_DEC.

**Notes:** If the digital gain ramping is enabled, (IN_STEP_RAMP_EN = 1), the volume increasing/decreasing ramp rates must be set to nonzero values. See Section 4.5.2 to configure the volume ramp rates.

The IN_RAMP_RATE_INC and IN_RAMP_RATE_DEC fields should not be changed while a volume ramp is in progress.

### 4.7.6 Auxiliary Device Control

Auxiliary device control is supported if the HGC SPI control interface is used, for details refer to Section 4.7.1. The host processor configures the auxiliary devices by writing to the respective AUXx_BIT_PATT fields. Each field contains the bit pattern to configure the respective external device as required.

**Note:** The bit pattern is a maximum of 32 bits (the size is configured using AUXx_BIT_PATT_LENGTH). If the bit pattern is 16 bits or less, it is stored in the AUXx_BIT_PATT_1 field. The MSB represents the first-transmitted bit of the pattern; one or more of the LSBs may be unused, depending on the size of the bit pattern. If the bit pattern is more than 16 bits, the remaining bits are stored in AUXx_BIT_PATT_0.

If the auxiliary bit patterns are updated, the new settings are latched internally and are not reflected in the SPI data output until a 1 is written to HGC_INIT_UPDATE. The host processor must confirm that the gain controller is idle (HGC_BUSY_STS = 0) before writing to HGC_INIT_UPDATE.

### 4.7.7 Initialization

Hybrid gain control must be initialized to ensure correct gain-ramping behavior. The host processor should configure the bit patterns and all gain fields for all channels—writing INx_UPDATE = 0 for each audio channel—and then write 1 to HGC_INIT_UPDATE to transmit the bit patterns and initialize the internal gain-control algorithms. If a pending update (INx_UPDATE = 1) is superseded by another update (INx_UPDATE = 0), the former is ignored. Note that the host processor must confirm that the gain controller is idle (HGC_BUSY_STS = 0) before writing to HGC_INIT_UPDATE.

**Note:** There is no zero-cross detection or transient masking when using HGC_INIT_UPDATE, so audible artifacts may occur. It is recommended to mute all audio channels (using INx_MUTE) to suppress any unintended transients.


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Writing to HGC_INIT_UPDATE has no effect if HGC_BUSY_STS = 1, indicating that gain updates are pending for one or more audio channels. The host processor can cancel any pending gain updates by writing 1 to HGC_ABORT—this can be used to return the controller to the idle state as quickly as possible, in readiness for initializing the system with a new configuration.

If the HGC_ABORT bit is written, the CS5312S does not become idle until it has finished applying the updates to the audio channel currently being processed. The host processor must always check the controller is idle (HGC_BUSY_STS = 0) before writing to HGC_INIT_UPDATE.

**Note:** Any gain updates that are canceled using the HGC_ABORT bit may result in an inconsistency between the register map and the respective gain settings. The HGC_ABORT bit should only be used as part of a control sequence that also uses HGC_INIT_UPDATE to apply a new configuration to all channels.

### 4.7.8 HGC Interrupts

The HGC function provides inputs to the interrupt controller, as described in Section 4.11. An interrupt is triggered if any of the following interrupt bits are set:

- HGC_SPI_ERROR_INT: indicates an invalid (zero-length) SPI transaction
- HGC_ABORT_ERROR_INT: the HGC operation has been aborted using the HGC_ABORT bit
- HGC_ERROR_INT: indicates a gain update error
- HGC_DONE_INT: indicates gain updates have completed successfully

These bits are latching fields which, once set, remain set until a 1 is written to the respective bit; these bits can be polled at any time or in response to the IRQ output signal being asserted.

## 4.8 Digital Filter Selection

The ADC input path incorporates a decimation filter and a high-pass filter. Four types of filter are supported:

- Fast roll-off, minimum phase
- Fast roll-off, linear phase
- Slow roll-off, minimum phase
- Slow roll-off, linear phase

The phase-responses are characterized as follows:

- The **minimum-phase** filters offer the lowest latency and an impulse response with no pre-ringing, at the expense of potential in-band phase distortion.
- The **linear-phase** filters have no phase distortion, but also higher latency and a symmetric impulse response.

The frequency-response options are characterized as follows:

- The **fast roll-off** filters maximize the audio signal bandwidth (as a function of the selected sample rate).The signal bandwidth and stopband attenuation are prioritized over impulse response and group delay.
- The **slow roll-off** filters are optimized for impulse response and group delay, with flat passband over the audible range to 20 kHz. The enhanced impulse response may improve perceived sound quality, especially for transient signal content.

The ADC input path supports fast roll-off filter options for all sample rates and slow roll-off filter options for 44.1 kHz—384 kHz sample rates.

In hardware control mode, the filter selection is determined by the CONFIG5 pin (see Section 4.2).

In software ($I^2C$/SPI) control mode, the decimation filter is selected using IN_FILTER_SEL; the high-pass filter is enabled using IN_HPF_EN.


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## 4.9 Audio Serial Port (ASP)

The multichannel ASP supports the output of digital audio samples from the CS5312S. The ASP can be configured as a primary or secondary interface, and supports I²S, left-justified, and TDM data formats.

Timing specifications for the ASP are described in Table 3-11. An option is supported to drive the output data (DOUT) on the rising or falling BCLK edge; driving on the rising edge (assuming noninverted BCLK polarity) can be used to support a larger load capacitance by increasing the time between the launching edge from the CS5312S and the sampling edge at the receiving device.

In hardware control mode, the ASP data format is determined by the CONFIG1 and CONFIG2 pins (see Section 4.2). In software (I²C/SPI) control mode, the ASP data format is configured using register fields.

In hardware mode, sample rates 16 kHz–192 kHz are supported (sample rates 16 kHz and 32 kHz are supported using autodetect in ASP Secondary Mode only). In software mode, sample rates 16 kHz–384 kHz are supported; sample rate 384 kHz is not supported by autodetect. The supported sample rates in ASP Primary Mode and ASP Secondary Mode are summarized in Table 4-13.

**Table 4-13. Supported Sample Rates in ASP Primary Mode and ASP Secondary Mode**

| | ASP Primary Mode | | ASP Secondary Mode | |
|---|---|---|---|---|
| **Sample Rate (kHz)** | **Hardware Control Mode** | **Software Control Mode** | **Hardware Control Mode** | **Software Control Mode** |
| 16–32 | — | Configurable using SAMPLE_RATE | Determined using autodetect only | Configurable using SAMPLE_RATE (autodetect available) |
| 44.1–192 | Determined by CONFIG1 pin | | | |
| 352.8, 384 | — | | — | Configurable using SAMPLE_RATE (autodetect not available) |

### 4.9.1 Primary and Secondary Operation

The ASP interface can operate as a primary or secondary interface. In the primary configuration, the BCLK and FSYNC signals are generated by the CS5312S. In the secondary configuration, the BCLK and FSYNC pins are inputs, allowing another device to drive the respective signals.

In ASP Secondary Mode, the external clocks (MCLK, BCLK, and FSYNC) must be derived from a common clock source and the active BCLK edge must be aligned with the falling MCLK edge.

If clocking is provided by the crystal oscillator and the CS5312S is operating in ASP Secondary Mode, then the FSYNC and the BCLK signals should be derived from the common clock source provided by the CS5312S MCLK output.

In hardware control mode, the ASP is configured as a primary or secondary interface using the CONFIG1 pin (see Section 4.2). In software control mode, the ASP primary/secondary configuration is selected using ASP_PRIMARY.

The ASP operation as a primary or secondary interface with MCLK as the clocking source is illustrated in Fig. 4-7 and Fig. 4-8.

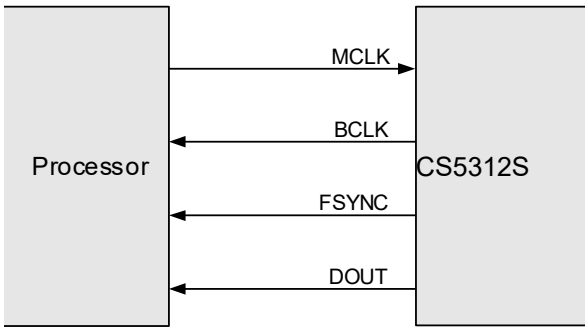


**Figure 4-7. Primary Mode, MCLK Clocking Source**

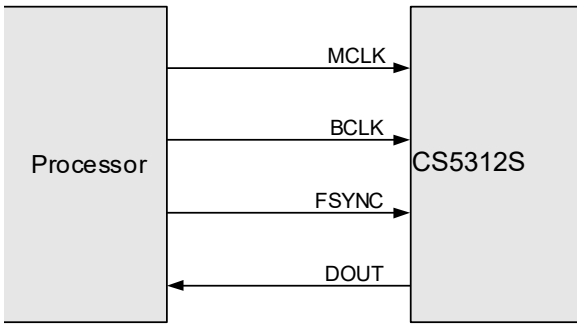


**Figure 4-8. Secondary Mode, MCLK Clocking Source**


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The ASP operation as a primary or secondary interface with a crystal as the clocking source is illustrated in Fig. 4-9 and Fig. 4-10.

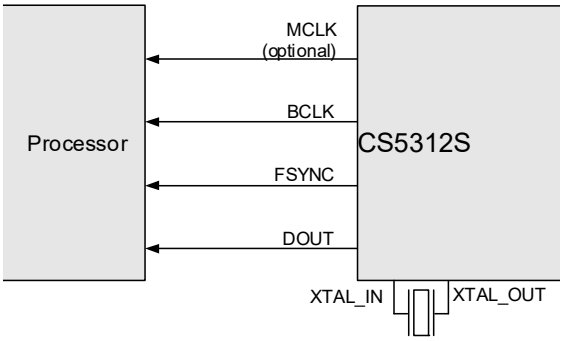


**Figure 4-9. Primary Mode, XTAL Clocking Source**

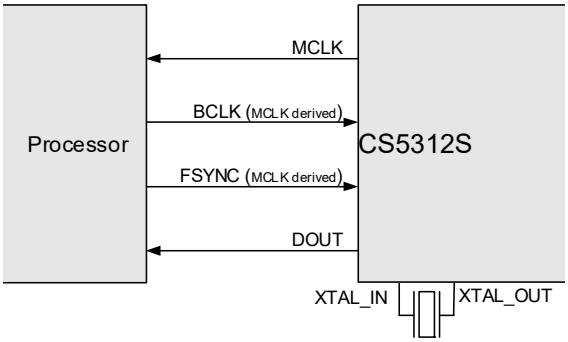


**Figure 4-10. Secondary Mode, XTAL Clocking Source**

## 4.9.2 ASP Data Formats

The ASP interface can be configured to operate in I²S, left-justified, or TDM data formats as illustrated in Fig. 4-11 through Fig. 4-13. The data-bit order is MSB first in each case; data words are encoded in 2's complement (signed, fixed-point) format. Each audio sample is allocated a time slot within the FSYNC frame.

- In I²S Mode, the MSB is valid on the second BCLK rising edge following an FSYNC transition. The other bits up to the LSB are valid on each successive BCLK cycle. Depending on word length, BCLK frequency, and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

  I²S Mode data format is shown in Fig. 4-11.

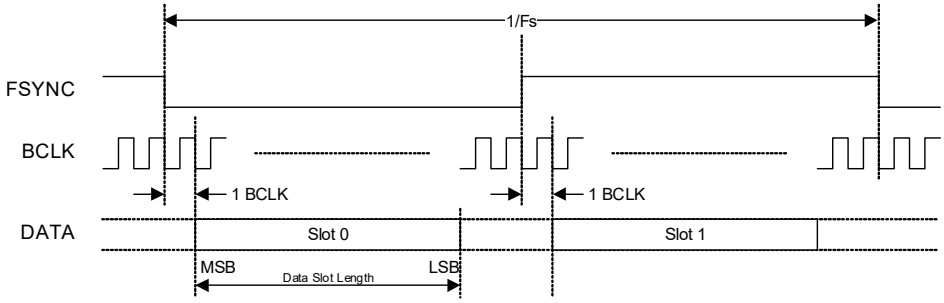


**Figure 4-11. I²S Data Format**

- In Left-Justified Mode, the MSB is valid on the first BCLK rising edge following an FSYNC transition. The other bits up to the LSB are valid on each successive BCLK cycle. Depending on word length, BCLK frequency, and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

  Left-Justified Mode data format is shown in Fig. 4-12.

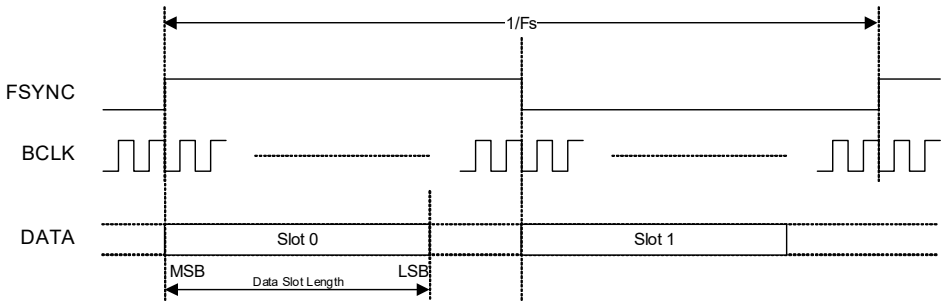


**Figure 4-12. Left-Justified Data Format**


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- In TDM Mode, if the ASP is configured in Secondary Mode, the MSB of the first channel is valid on the second BCLK rising edge following a rising FSYNC edge. The other bits up to the LSB are valid on each successive BCLK cycle.

  If the ASP is configured in Primary Mode, the FSYNC signal can be configured as a pulse (default) or a square wave (with a 50% duty cycle). If the FSYNC signal is configured as a pulse, the MSB of the first channel is valid on the second BCLK rising edge following a rising FSYNC edge. The other bits up to the LSB are valid on each successive BCLK cycle.

  In ASP Secondary Mode and in ASP Primary Mode with the FSYNC signal configured as a pulse, the subsequent channels follow immediately after the first channel. The pulse duration can be anything less than 1/Fs, provided the falling edge of the frame pulse occurs at least one BCLK period before the rising edge of the next frame pulse. Depending on word length, BCLK frequency, and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

  TDM Mode data format in ASP Secondary Mode and ASP Primary Mode with FSYNC configured as a pulse is shown in Fig. 4-13.

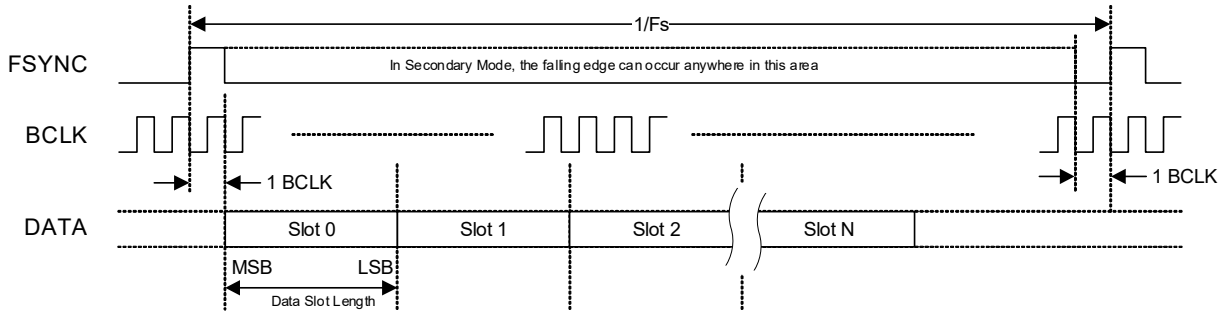


**Figure 4-13. TDM Data Format Primary Mode (FSYNC = Pulse) and Secondary Mode**

  In ASP Primary Mode with the FSYNC signal configured as a square wave, the slots are aligned with both rising and falling edges of FSYNC and half of the available slots occur within each phase of the FSYNC cycle. The total number of available slots is determined by the sample rate, as described in Table 4-15.

- The MSB of the first channel in each phase of the FSYNC cycle is valid on the second BCLK rising edge following the rising and falling FSYNC edge respectively. The other bits up to the LSB are valid on each successive BCLK cycle. Depending on word length, BCLK frequency, sample rate, and number of available slots, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

  TDM Mode data format in ASP Primary Mode with FSYNC configured as a square wave is shown in Fig. 4-14.

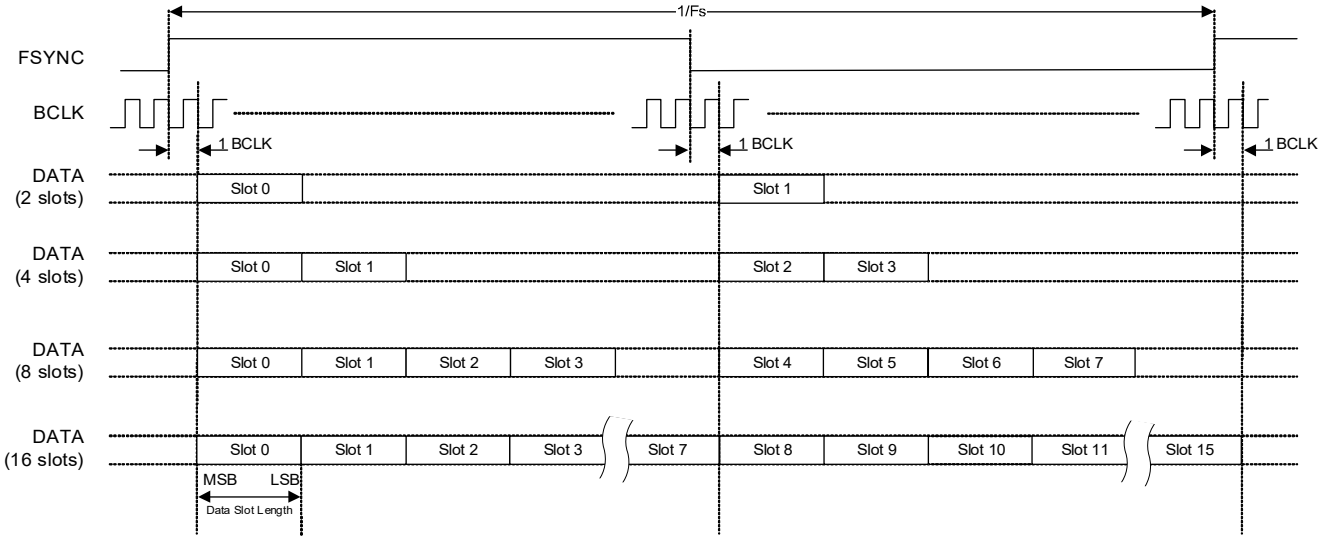


**Figure 4-14. TDM Data Format Primary Mode (FSYNC = Square Wave)**


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### 4.9.3 ASP Configuration

In hardware control mode, the ASP data format is determined by the CONFIG1 and CONFIG2 pins (see Section 4.2).

In software control mode, the ASP data format is configured using SAMPLE_RATE, and ASP_FORMAT. If ASP Primary Mode is selected (see Section 4.9.1), the BCLK frequency is configured using ASP_BCLK_FREQ and the FSYNC waveform type (pulse or square wave) is configured using ASP_FSYNC_TYPE.

In software control mode, the BCLK polarity is selected using ASP_BCLK_INV. The polarity selection is valid in Primary and Secondary Modes, and determines whether the data is valid for sampling on the rising edge or the falling edge.

The BCLK polarity is illustrated in Fig. 4-15 and Fig. 4-16. In hardware control mode, the BCLK polarity is assumed to be noninverted.

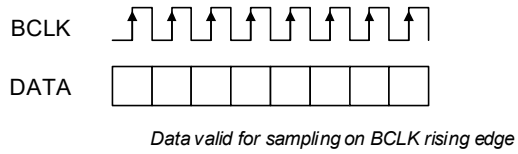


**Figure 4-15. Noninverted BCLK**

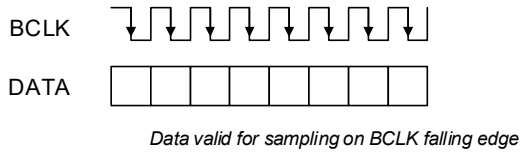


**Figure 4-16. Inverted BCLK**

In TDM Mode, the two data-format options are supported as follows:

- TDM Mode—minimum slots. The ASP data format is configured to support two slots. This mode allows the BCLK rate to be as low as possible, equating to a minimum of 128 BCLK cycles per audio sample at a minimum sample rate of 64 Fs.
- TDM Mode—maximum time slots. The ASP data format is configured to support the maximum number of time slots for the applicable BCLK rate. The mode is designed for the maximum BCLK rate (22.5792 MHz for sample rates of 44.1, 88.2, 176.4, and 352.8 kHz, or 24.576 MHz for sample rates of 16, 32, 48, 96, 192, and 384 kHz), enabling the maximum possible bandwidth on the ASP data bus to be shared with other devices.

If the ASP is configured for TDM Mode with maximum time slots, the output data (DOUT) can be driven either on the rising or falling BCLK edge. Driving on the rising edge (assuming noninverted BCLK polarity) can be used to support a larger load capacitance by increasing the time between the launching edge from the CS5312S and the sampling edge at the receiving device.

Note that the ASP timing options are dependent on the behavior of the receiving device. It is assumed, for noninverted BCLK, the data is sampled on the rising BCLK edge. Similarly, for inverted BCLK, it is assumed the data is sampled on the falling BCLK edge.

The DOUT drive options for half-cycle and full-cycle mode are described in Table 4-14. In full-cycle mode, the output data is driven on the same BCLK edge as it is sampled (i.e., one full BCLK cycle before the sampling edge). In half-cycle mode, the output data is driven on the opposite BCLK edge as it is sampled (i.e. one half BCLK cycle before the sampling edge), this is also illustrated in Table 3-11.

**Table 4-14. TDM Mode (Maximum Time Slots)—DOUT Drive Timing**

| TDM Mode [1] | BCLK Polarity [2] | DOUT Launching (Drive) Edge | DOUT Latching (Sampling) Edge |
|---|---|---|---|
| Half-cycle | Noninverted | BCLK falling | BCLK rising |
| | Inverted | BCLK rising | BCLK falling |
| Full-cycle | Noninverted | BCLK rising | BCLK rising |
| | Inverted | BCLK falling | BCLK falling |

1. The TDM variant is selected using the CONFIG2 pin (in hardware control mode) or ASP_FORMAT (in software control mode).
2. The BCLK polarity is selected using ASP_BCLK_INV in software control mode. In hardware control mode, the polarity is assumed noninverted.


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The ASP configuration depends on the sample rate and the selected data format as described in Table 4-15.

**Table 4-15. ASP Data Format**

| ASP Format [1] | ASP Sample Rate [2,3] | Time Slots per Frame [4] | BCLK Rate[5,6] |
|---|---|---|---|
| I²S, Left-Justified | 16 kHz | 2 | BCLK ≥ 64×Fs[7] |
| | 32 kHz | | BCLK ≥ 64×Fs[8] |
| | 44.1 kHz, 48 kHz | | BCLK ≥ 64×Fs |
| | 88.2 kHz, 96 kHz | | BCLK ≥ 64×Fs |
| | 176.4 kHz, 192 kHz | | BCLK ≥ 64×Fs |
| | 352.8 kHz, 384 kHz | | BCLK ≥ 64×Fs |
| | Autodetect (16 kHz–192 kHz) | | BCLK ≥ 64×Fs |
| TDM—minimum time slots | 16 kHz | | BCLK ≥ 64×Fs[7] |
| | 32 kHz | | BCLK ≥ 64×Fs[8] |
| | 44.1 kHz, 48 kHz | | BCLK ≥ 64×Fs |
| | 88.2 kHz, 96 kHz | | BCLK ≥ 64×Fs |
| | 176.4 kHz, 192 kHz | | BCLK ≥ 64×Fs |
| | 352.8 kHz, 384 kHz | | BCLK ≥ 64×Fs |
| | Autodetect (16 kHz–192 kHz) | | BCLK ≥ 64×Fs |
| TDM—maximum time slots | 16 kHz | 16 | BCLK ≥ 512×Fs[7] |
| | 32 kHz | | BCLK ≥ 512×Fs[8] |
| | 44.1 kHz, 48 kHz | | BCLK = 512×Fs |
| | 88.2 kHz, 96 kHz | 8 | BCLK = 256×Fs |
| | 176.4 kHz, 192 kHz | 4 | BCLK = 128×Fs |
| | 352.8 kHz, 384 kHz | 2 | BCLK = 64×Fs |
| | Autodetect (16 kHz–192 kHz) | 4 | BCLK ≥ 128×Fs |

1. The ASP format is selected using the CONFIG2 pin (in hardware control mode) or ASP_FORMAT (in software control mode).
2. The sample rate is selected using the CONFIG1 pin (in hardware control mode) or SAMPLE_RATE (in software control mode).
3. Sample rates 16 kHz–192 kHz are supported in hardware and software control modes; sample rate 384 kHz is supported in software control mode only.
4. Time slots per frame is the number of data-sample time slots supported on the DOUT pin.
5. The BCLK rate must be a constant integer multiple of the sample rate (Fs).
6. In ASP Primary Mode (hardware control), the BCLK frequency is the minimum specified rate. In ASP Primary Mode (software control), the BCLK frequency is configured using ASP_BCLK_FREQ.
7. In ASP Primary Mode, the specified minimum BCLK frequency for 16 kHz sample rate is not supported. The available options correspond to 192×Fs, 384×Fs, 768×Fs, or 1536×Fs
8. In ASP Primary Mode, the specified minimum BCLK frequency for 32 kHz sample rate is not supported. The available options correspond to 96×Fs, 192×Fs, 384×Fs, or 768×Fs.

The ASP data format in I²S, Left-Justified, and TDM interface modes as illustrated in Fig. 4-17 through Fig. 4-20. Refer to Table 4-15 for the applicable definition.

- If I²S data format is selected, the ASP supports audio channels 1–2 as shown in Fig. 4-17. The minimum BCLK rate is 64×Fs (where Fs is the sample rate). In ASP Primary Mode, the minimum BCLK rate of 64×Fs is not supported for sample rates of 16 kHz or 32 kHz. A higher BCLK frequency can be used, resulting in unused BCLK cycles between the LSB of one sample and the MSB of the next.

  The output data is provided on ASP_DOUT.

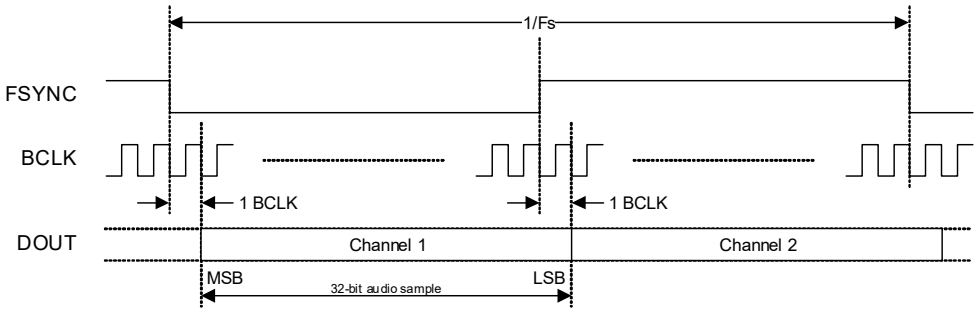


**Figure 4-17. I²S Data Format**


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- If Left-Justified data format is selected, the ASP supports audio channels 1–2 as shown in Fig. 4-18. The minimum BCLK rate is 64×Fs (where Fs is the sample rate). In ASP Primary Mode, the minimum BCLK rate of 64×Fs is not supported for sample rates of 16 kHz or 32 kHz. A higher BCLK frequency can be used, resulting in unused BCLK cycles between the LSB of one sample and the MSB of the next.

  The output data is provided on ASP_DOUT.

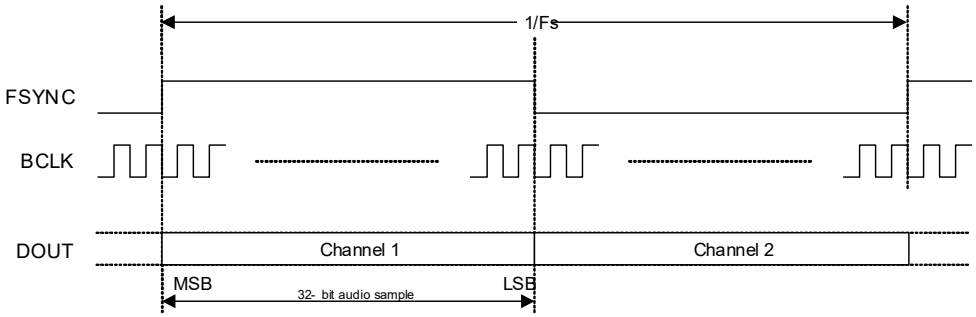


**Figure 4-18. Left-Justified Data Format**

- In TDM Mode, the FSYNC frame is configured for 2, 4, 8, or 16 slots as specified in Table 4-15.

  In 4-, 8-, and 16-slot modes, the slot assignment for audio channels 1–2 is selected using the CONFIG3 pin (in hardware control mode—see Section 4.2) or else using ASP_TDM_SLOT (in software control mode). In 2-slot modes, the default slot assignment (slots 0–1) should be selected.

  The BCLK rate is related to the sample rate (Fs) as described in Table 4-15. Where applicable, the BCLK rate can be higher than the stated minimum, resulting in additional unused BCLK cycles between the last slot in the frame and the start of the next frame.

  The ASP_DOUT pin is high impedance if the CS5312S is not transmitting data, allowing other devices on the bus to transmit data during any unused time slots.

  The output data is provided on ASP_DOUT.

  An example of the 4-slot TDM format in ASP Secondary Mode and in ASP Primary Mode with the FSYNC signal configured as a pulse is shown in Fig. 4-19. In this example, audio channels 1–2 occupy TDM slots 0–1 respectively.

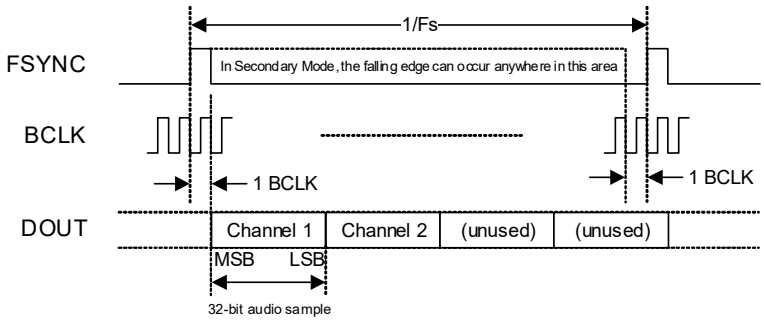


**Figure 4-19. TDM Data Format, 4-Slot Example (FSYNC = Pulse)**


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An example of the 4-slot TDM format in ASP Primary Mode with the FSYNC signal configured as a square wave is shown in Fig. 4-20. In this example, audio channels 0 and 1 occupy TDM slots 0 and 1 in the high (Logic 1) phase of the FSYNC signal, TDM slot 0 and 1 in the low (Logic 0) phase of the FSYNC signal are unused.

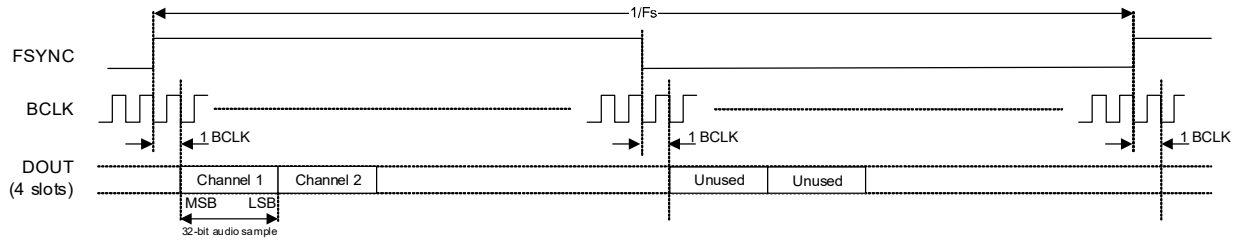


**Figure 4-20. TDM Data Format, 4-Slot Example (FSYNC = Square Wave)**

## 4.10 I2C/SPI Control Port

The CS5312S incorporates a control port, supporting I2C or SPI modes of operation; this is selected using CONFIG1, as described in Table 4-1. If the SPI control interface is required, it is recommended to use a pull-up resistor of 100 kΩ. In software control mode, the CS5312S is configured by writing to control registers using the control port.

The control port is automatically configured in I2C mode or SPI mode following the first valid I2C/SPI activity detected after power-on or hardware reset.

### 4.10.1 I2C Control Port

The I2C control port is supported using the following pins, which must be configured for the I2C function if required:

- CONFIG2/SPI_SDI/I2C_SDA
- CONFIG3/SPI_SDO/I2C_SCL

The CS5312S is a target device on the I2C bus—SCL is a clock input, while SDA is a bidirectional data pin. To allow arbitration of multiple targets (and/or multiple controllers) on the same interface, the CS5312S transmits Logic 1 by tristating the SDA pin, rather than pulling it high. An external pull-up resistor is required to pull the SDA line high so that the Logic 1 can be recognized by the controller.

In order to allow many devices to share a single two-wire control bus, every device on the bus has a unique 8-bit device address (this is not the same as the address of each register in the CS5312S). The LSB of the device address is the read/write bit; this bit is set to Logic 1 for read and Logic 0 for write.

The I2C device address is configured using the CONFIG1 pin as described in Table 4-16.

**Table 4-16. I2C Address Selection—CONFIG1 pin**

| Pin Configuration | | I2C Address |
|---|---|---|
| Pull-up to VDD_IO1 | 0 kΩ | 0x26 (write), 0x27 (read) |
| | 4.7 kΩ | 0x24 (write), 0x25 (read) |
| | 22 kΩ | 0x22 (write), 0x23 (read) |
| | 100 kΩ | 0x20 (write), 0x21 (read) |

The host device indicates the start of data transfer with a high-to-low transition on SDA while SCL remains high. This indicates that a device address and subsequent address/data bytes follow. The CS5312S responds to the start condition and shifts in the next 8 bits on SDA (8-bit device address, including read/write bit, MSB first). If the device address received matches the device address of the CS5312S, the CS5312S responds by pulling SDA low on the next clock pulse (ACK). If the device address is not recognized or the R/W bit is set incorrectly, the CS5312S returns to the idle condition and waits for a new start condition.


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If the device address matches the device address of the CS5312S, the data transfer continues. The controller indicates the end of data transfer with a low-to-high transition on SDA while SCL remains high. After receiving a complete address and data sequence the CS5312S returns to the idle state and waits for another start condition. If a start or stop condition is detected out of sequence at any point during data transfer (i.e., SDA changes while SCL is high), the device returns to the idle condition.

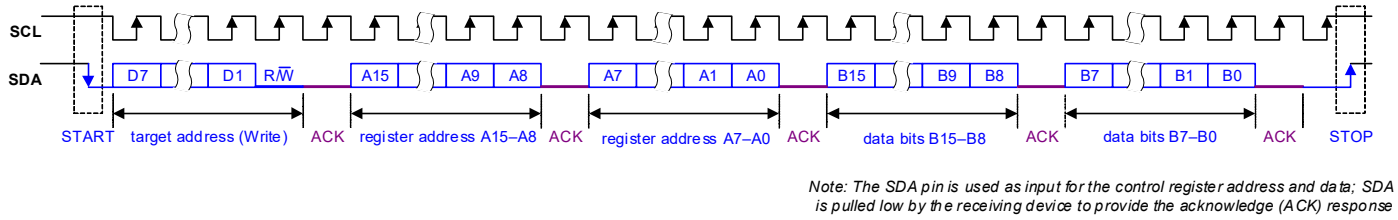
The I2C interface uses a 16-bit register address and 16-bit data words. The register address must be aligned to a 16-bit word boundary (i.e., the LSB must be 0). The full I2C message protocol also includes a device address, a read/write bit, and other signaling bits (see Fig. 4-21 and Fig. 4-22).

The CS5312S supports the following read and write operations:

- Single write
- Single read
- Multiple write
- Multiple read

Continuous (multiple) read and write modes allow register operations to be scheduled faster than is possible with single register operations. In these modes, the CS5312S automatically increments the register address after each data word. Successive data words can be input/output every two data bytes.

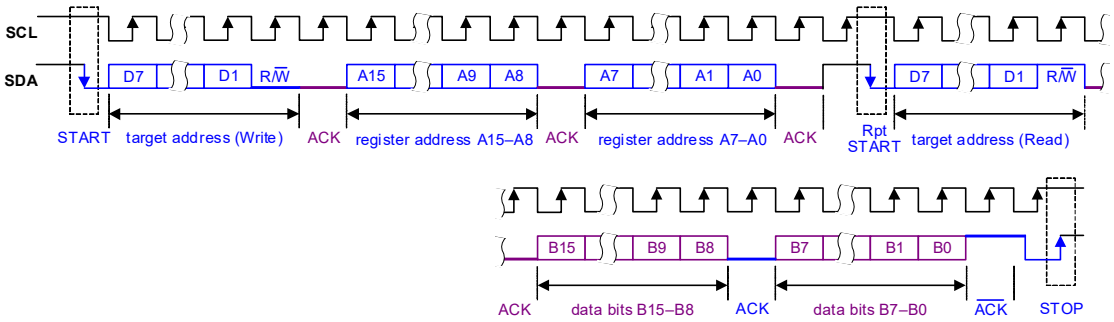
The I2C protocol for a single, 16-bit register write operation is shown in Fig. 4-21.




*Note: The SDA pin is used as input for the control register address and data; SDA is pulled low by the receiving device to provide the acknowledge (ACK) response*

**Figure 4-21. Control Interface I2C Register Write**

The I2C protocol for a single, 16-bit register read operation is shown in Fig. 4-22.




*Note: The SDA pin is driven by both the controller and target devices in turn to transfer target address, register address, data and ACK responses*

**Figure 4-22. Control Interface I2C Register Read**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The control interface also supports other register operations; the interface protocol for these operations is shown in Fig. 4-23 through Fig. 4-26. The terminology used in the following figures is detailed in Table 4-17.

**Table 4-17. Control Interface (I2C) Terminology**

| Terminology | Description |
|---|---|
| S | Start condition |
| Sr | Repeated start |
| A | Acknowledge (SDA low) |
| $\overline{A}$ | No Acknowledge (SDA high) |
| P | Stop condition |
| R/$\overline{W}$ | Read/not Write: 0 = Write, 1 = Read |
| [White field] | Data flow from bus controller to CS5312S |
| [Gray field] | Data from CS5312S to bus controller |

Fig. 4-23 shows a single register write to a specified address.

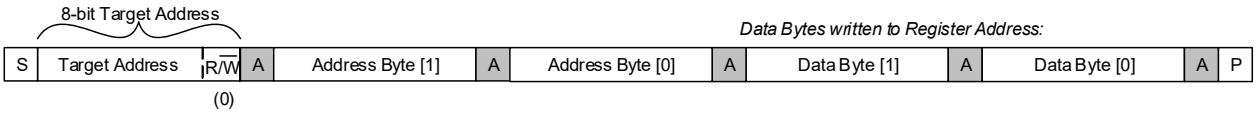


**Figure 4-23. Single-Register Write to Specified Address**

Fig. 4-24 shows a single register read from a specified address.

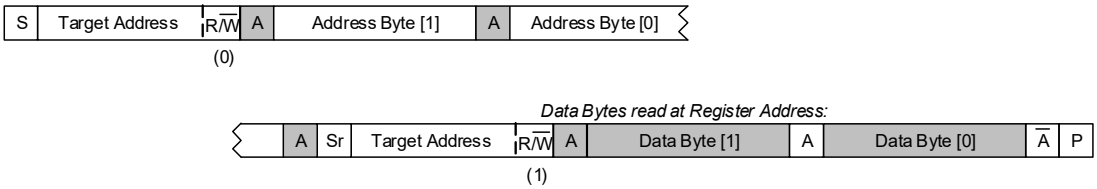


**Figure 4-24. Single-Register Read from Specified Address**

Fig. 4-25 shows a multiple register write to a specified address.

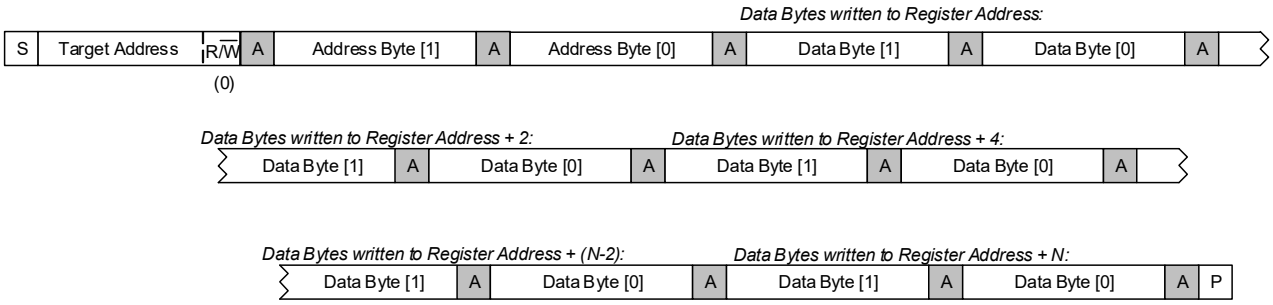


**Figure 4-25. Multiple-Register Write to Specified Address**


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Fig. 4-26 shows a multiple register read from a specified address.

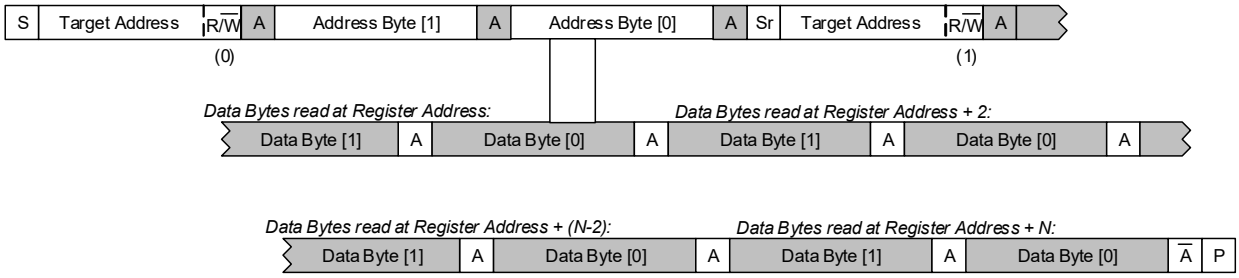


**Figure 4-26. Multiple-Register Read from Specified Address**

## 4.10.2 SPI Interface

The SPI interface is supported using the following pins, which must be configured for the SPI function if required:

- CONFIG1/$\overline{\text{SPI_CS}}$
- CONFIG2/SPI_SDI/I2C_SDA
- CONFIG3/SPI_SDO/I2C_SCL
- CONFIG5/SPI_SCK

To ensure that the control port is inactive prior to use, $\overline{\text{SPI_CS}}$ must be deasserted (i.e., Logic 1) during device startup; $\overline{\text{RESET}}$ must remain asserted (i.e., Logic 0) until $\overline{\text{SPI_CS}}$ is deasserted (i.e., Logic 1), timing information is provided in Table 3-10.

The SDI (data-input) pin supports the following behavior:

- In write operations (R/$\overline{\text{W}}$ = 0), the SDI pin input is driven by the controlling device.
- In read operations (R/$\overline{\text{W}}$ = 1), the SDI pin is ignored following receipt of the valid register address.

The SDO (data-output) pin supports the following behavior:

- If $\overline{\text{CS}}$ is asserted (Logic 0), the SDO output is actively driven when outputting data and is high impedance at other times. If $\overline{\text{CS}}$ is not asserted, the SDO output is high impedance.
- The high-impedance state of the SDO output allows the pin to be shared with other peripheral devices.
- The output (SDO) data bit is available to the host device at the rising edge of SCK. See Table 3-13 for timing information.

The SPI interface uses a 15-bit register address and 16-bit data words. The full SPI message protocol also includes a read/write bit and a 16-bit padding phase (see Fig. 4-27 and Fig. 4-28).

Continuous read and write modes enable multiple register operations to be scheduled faster than is possible with single register operations. In these modes, the CS5312S automatically increments the register address at the end of each data word, for as long as $\overline{\text{CS}}$ is held low and SCK is toggled. Successive data words can be input/output every 16 clock cycles.

The SPI protocol is shown in Fig. 4-27 and Fig. 4-28.


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Fig. 4-27 shows a single register write to a specified address.

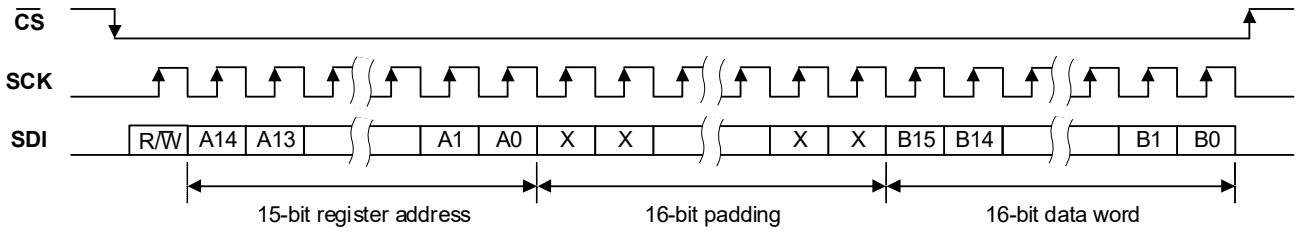


**Figure 4-27. Control Interface SPI Register Write**

Fig. 4-28 shows a single register read from a specified address.

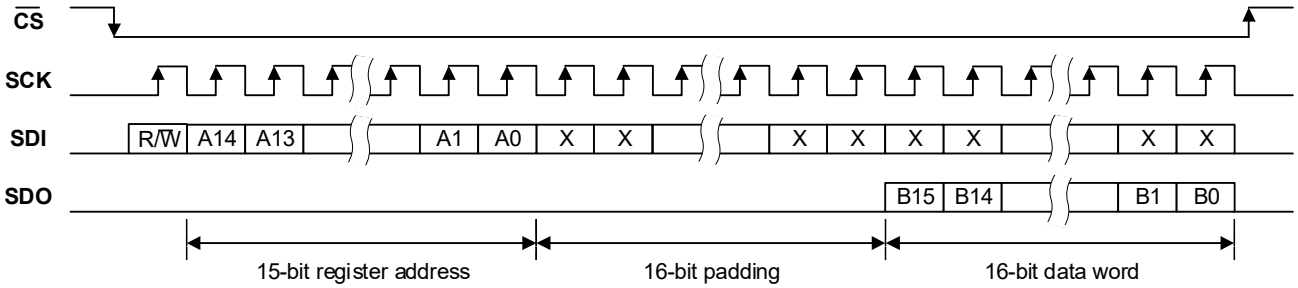


**Figure 4-28. Control Interface SPI Register Read**

Fig. 4-29 shows a multiple register write to a specified address.

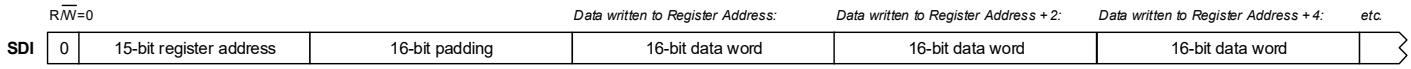


**Figure 4-29. Multiple-Register Write to Specified Address**

Fig. 4-30 shows a multiple register read from a specified address.

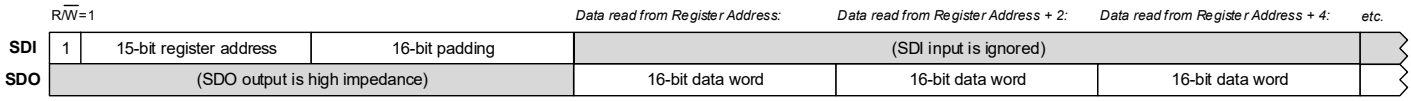


**Figure 4-30. Multiple-Register Read from Specified Address**


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## 4.11 Interrupts

The CS5312S incorporates an interrupt controller for monitoring event conditions. Inputs to the interrupt controller include clip warning, virtual PAD, and HGC warning/error conditions.

Any of these input conditions can be used to assert the IRQ output signal. The IRQ signal can be configured as an output on different pins, as described in Table 4-18.

**Table 4-18. IRQ Event Logic Output Pins**

| Pin Name | Power Supply | Control Field | Notes |
|---|---|---|---|
| GPIO1 [1] | VDD_IO2 | GPIO1_IRQ_EN | IRQ not supported if pin is configured for virtual PAD or GPIO-based HGC external gain control. |
| $\overline{\text{HGC_CS}}$/GPIO2 [1] | VDD_IO2 | GPIO2_IRQ_EN | IRQ not supported if pin is configured for virtual PAD or SPI- or GPIO-based HGC external gain control. |
| CONFIG4/CH_IDLE | VDD_IO1 | CONFIG4_IRQ_EN | If pin is configured for signal-activity detection, this pin should not be used for IRQ. |
| CONFIG5/SPI_SCK | VDD_IO1 | SPI_SCK_IRQ_EN | IRQ not supported if SPI control interface is used. |

1. The GPIO logic levels are referenced to the VDD_IO2 domain; level shifting may be required if connecting to a host interface operating at a different level (see Table 3-8 for details).

An interrupt register bit, x_INT, is associated with each interrupt input, indicating that the respective event has been detected. The interrupt bits are latching fields which, once set, remain set until a 1 is written to the respective bits. The interrupt register bits can be polled at any time or in response to the IRQ output signal being asserted.

A status bit, x_STS, is provided to indicate the current status of the clip warning and virtual PAD inputs.

Mask bits, x_MASK, are provided for each input condition, to enable or disable the respective functions from contributing to the interrupt logic output. The interrupt register bits (x_INT) remain valid—even if masked—but the masked interrupts do not cause the interrupt logic output to be asserted.

The output can be either CMOS driven or open drain; this is selected using IRQ_OP_CFG.

- If the output is configured as CMOS driven, the IRQ output signal is active high, i.e., Logic 1 if one or more unmasked interrupt is asserted.
- If the output is configured as open drain, the IRQ output signal is active low, i.e., Logic 0 if one or more unmasked interrupt is asserted.

The IRQ signal represents the logical OR of the unmasked interrupt registers. The IRQ output remains asserted until all of the associated interrupts have been either masked or reset.

The IRQ status is indicated using IRQ_STS; this bit is set if one or more unmasked interrupt is asserted.

## 4.12 Device ID

The device ID, and other associated data, can be read from the control fields listed in Table 4-19.

**Table 4-19. Device ID**

| Label | Description |
|---|---|
| DEVID_0 | Lower bytes of the Device ID |
| DEVID_1 | Upper bytes of the Device ID |
| AREVID | All-layer device revision |
| MTLREVID | Metal-layer device revision |


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# 5 Applications

## 5.1 Input Buffer Circuit

The analog input channels are supported using external buffer circuits. A typical buffer circuit comprising a high-pass filter and anti-alias filter is shown in Fig. 5-1. The typical buffer circuit shown produces a full-scale (0 dBFS) output from a 2 $V_{RMS}$ differential input.

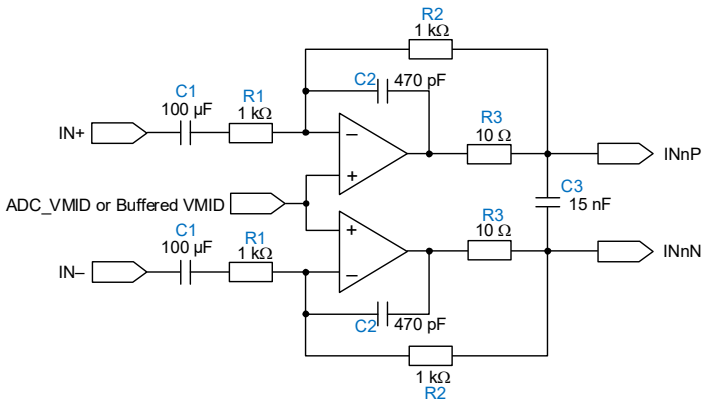


**Figure 5-1. Differential Input Buffer Circuit**

The high-pass filter is provided by the AC-coupling capacitor, C1 and series resistor, R1. Using the values shown, the –3 dB cut-off frequency ($F_C$) can be calculated using the following equation:

$$F_C = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi \times 1000 \times (100 \times 10^{-6})} = 1.59\ \text{Hz}$$

The anti-alias filter is provided by the operational amplifier and associated feedback components. The objective is to provide a flat passband for the audio input bandwidth, and sufficient attenuation at the ADC-modulator sample frequency. The low output impedance of the circuit minimizes the distortion of the signal path.

The typical filter shown provides an approximated –3 dB cut-off frequency of 424 kHz, suitable for the highest CS5312S sample rate of 384 kHz. The attenuation slope of –12 dB/octave results in 48 dB attenuation at the ADC-modulator sample frequency of 6.144 MHz.

The –3 dB cut-off frequency is approximated by the following equation:

$$F_C = \frac{1}{2\pi\sqrt{R_2 R_3 C_2 2 C_3}} = \frac{1}{2\pi\sqrt{1000 \times 10 \times 470 \times 10^{-12} \times 2 \times 15 \times 10^{-9}}} = 424\ \text{kHz}$$

The gain of the input buffer is set by R1 and R2. The gain should be configured to provide a full-scale signal of 2 $V_{RMS}$ at the input to the CS5312S. The values shown in Fig. 5-1 provide a ratio of 1; in this configuration, the buffer supports a full-scale input of 2 $V_{RMS}$.

The ADC_VMID reference is provided as an output from the CS5312S. The ADC_VMID current (arising from capacitor leakage and the input-buffer circuit) must be less than the maximum output current specified in Table 3-9. If a larger current is required, an external VMID buffer should be used; an example of a buffered VMID circuit is provided in Table 3-9.

### 5.1.1 Unused Input Pins

The recommended input buffer circuit (see Fig. 5-1) provides a differential connection to the input pins INnP and INnN. Alternative input-buffer circuits may use only a single-ended connection to INnP or INnN. If a single-ended input configuration is used, the unused input pin must be connected to a buffered VMID reference, see Table 3-9 for a buffered VMID circuit. If one, or more, input channel is not used (disabled), the respective unused input pin INnP or INnN should be floating (no connection).


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## 5.2 PCB Layout Guidelines

The recommended layout guidelines are provided in this section. Typical external components are described in Section 2.

### 5.2.1 General Layout Guidelines

The following general guidelines should be followed:

- Digital signals should be supported using a controlled 50 Ω characteristic impedance.
- Avoid routing digital signals between power planes on an adjacent layer.
- Avoid routing analog and digital signals next to each other.
- If a signal crosses another signal on an adjacent layer, they should cross perpendicularly to prevent coupling.
- Signals must not cross power-plane shapes or ground cut-offs on an adjacent layer.

### 5.2.2 Component Placement

The following guidelines on component placement should be followed:

- Power supply decoupling capacitors should be placed as close as possible to the CS5312S, with a strong connection to the ground plane.
- The voltage reference (ADC_VMID) capacitors and LDO filter (LDO_VD_FILT) capacitor should be placed close to the CS5312S, with a strong connection to the ground plane.

### 5.2.3 Ground Routing

The following guidelines are recommended for ground connection:

- The ground paddle of the CS5312S should be connected to the ground plane with at least five vias.
- The ground paddle should not be connected directly to any pin.

### 5.2.4 VDD_A Routing

The following guidelines are recommended for the VDD_A supply:

- VDD_A1 and VDD_A2 should be star-connected to a 3.3 V power plane.
- Decoupling capacitors (0.01 µF and 4.7 µF) should be provided for each supply pin (VDD_A1 and VDD_A2), as shown in Section 2.

### 5.2.5 ADC_FILT Routing

- Decoupling capacitors (0.1 µF, 1 µF, and 100 µF) should be connected to the ADC_FILT_P and ADC_FILT_N pins, as shown in Section 2.
- The 0.1 µF capacitor should be placed closest to the CS5312S, then the 1 µF capacitor, then the 100 µF capacitor.
- The ADC_FILT_N trace should be connected to ground after the 100 µF capacitor.
- The ADC_FILT_P trace should be star-connected to VDD_A2 using a 1 Ω resistor placed after the 100 µF capacitor.

## 5.3 Recommended Components

To achieve the specified performance characteristics, the choice of external components should observe the following recommendations:

- Capacitors should be stable dielectric types, such as C0G (NP0) or electrolytic.
- Resistors should be low value where possible, to minimize thermal noise.


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- Low-noise operational amplifiers should be used, such as Texas Instruments OPA1656. The operational amplifiers should meet the minimum performance requirements noted in Table 5-1.

**Table 5-1. Op-Amp Specification**

| Parameter | Specification |
|---|---|
| Input noise | <5 nV/√Hz |
| Unity gain bandwidth | >15 MHz |
| Slew rate | 5 V/µs |
| Total harmonic distortion plus noise (THD+N) | <–128 dB |

### 5.3.1 Crystal Component Selection

The crystal oscillator (see Section 4.4) uses an external crystal to generate the timing reference. Load capacitors are connected to the crystal as shown in Fig. 5-2. A series resistor ($R_S$) may also be required to configure the drive level for the selected crystal.

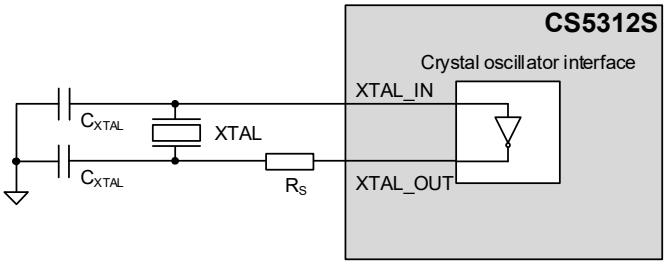


**Figure 5-2. Crystal Oscillator Connection**

The suitability of the selected crystal is determined by whether the gain margin and drive level are within the valid operating limits of the crystal. The gain margin and drive level can be calculated as a function of the transconductance of the crystal interface.

The transconductance of the crystal interface is dependent on the VDD_IO2 operating voltage as described in Table 3-10.

The recommended sequence for crystal component selection is as follows:

1. **Crystal selection.** The CS5312S is compatible with a wide variety of crystal components, including the KC3225Z series of oscillators.
2. **Capacitor selection.** Capacitors should be selected according to the crystal manufacturer's specification for load capacitance ($C_L$). The recommended value for each $C_{XTAL}$ capacitor is 2 × $C_L$.
3. **Series resistor.** In the first instance, assume the series resistor Rs is not required (0 Ω).
4. **Gain margin calculation.** The gain margin can be calculated from the transconductance of the crystal interface and the series resistor $R_S$, together with the crystal characteristics. If the required gain margin is less than 5, a different crystal selection must be made (Step 1).

   The gain margin is calculated as follows: $\text{Gain Margin} = \dfrac{\text{Transconductance}}{4 \times (\text{ESR} + R_S) \times (2\pi \times f_{XTAL})^2 \times (C_0 + C_L)^2}$

   where:

   Transconductance = transconductance of the crystal interface (S)

   ESR = equivalent series resistance (ESR) of the crystal (Ω)

   $R_S$ = series resistance (Ω)

   $f_{XTAL}$ = resonant frequency of the crystal (Hz)

   $C_L$ = load capacitance of the crystal (F)

   $C_0$ = shunt capacitance of the crystal (F)
5. **Drive level calculation.** The drive level can be calculated using the crystal characteristics and the operating voltage. The operating voltage (peak voltage across the crystal) can be determined using measurement or else by


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simulation. If the drive level exceeds the maximum level for the crystal, adjust the series resistor $R_S$ to meet the required specification. Increasing $R_S$ results in a lower voltage across the crystal and a decrease in drive level.

If the series resistor is adjusted, the gain margin must now be recalculated (Step 4). It is recommended to find the minimum series resistance that meets the required gain margin and drive level.

The drive level (W) is calculated as follows: $\text{Drive Level} = 2 \times ESR \times (\pi \times f_{XTAL} \times V \times (C_L + C_0))^2$

where:

ESR = equivalent series resistance (ESR) of the crystal (Ω)

$f_{XTAL}$ = resonant frequency of the crystal (Hz)

V = Peak voltage across the crystal (V)

$C_L$ = load capacitance of the crystal (F)

$C_0$ = shunt capacitance of the crystal (F)

The sequence for crystal component selection is illustrated in Fig. 5-3.

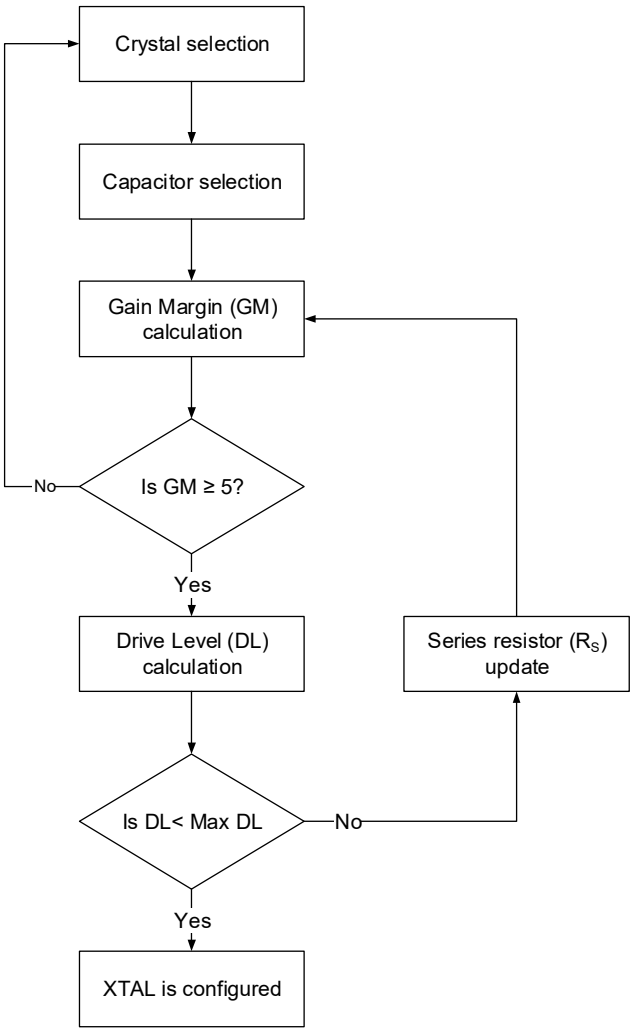


**Figure 5-3. Crystal Oscillator Component Selection**


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# 6 Register Quick Reference

This section gives an overview of the control port registers. Refer to the following bit definition tables for bit assignment information.

This register view is for the CS5312S.

- The register field default values are established upon the deassertion of the $\overline{\text{RESET}}$ pin or following soft reset.
- A "—" represents a reserved field/access type.
- The reserved field values must not be modified.
- The registers are 16 bits wide, and only word transactions are allowed.
- All visible fields are read/write except where indicated with the following shading:

Read/write access  Read-only access  Write-only access

**Table 6-1. Block Base Addresses**

| Base Address | Block Name | Register Quick Reference | Register Description Reference |
|---|---|---|---|
| 0x0000 0000 | **DEVID** | Section 6.1 | Section 7.1 |
| 0x0000 0040 | **CONFIG** | Section 6.2 | Section 7.2 |
| 0x0000 0080 | **INPUT_PATH** | Section 6.3 | Section 7.3 |
| 0x0000 2000 | **HGC** | Section 6.4 | Section 7.4 |
| 0x0000 3D00 | **PIN_CONFIG** | Section 6.5 | Section 7.5 |
| 0x0000 3E00 | **IRQ_CONFIG** | Section 6.6 | Section 7.6 |

## 6.1 DEVID

| Address | Register | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x0000 0000 | DEVID_0 | DEVID_0 | | | | | | | | | | | | | | | |
| p. 55 | | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| 0x0000 0002 | DEVID_1 | DEVID_1 | | | | | | | | | | | | | | | |
| p. 55 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 0x0000 0004 | REVID | — | | | | | | | | AREVID | | | | MTLREVID | | | |
| p. 55 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 0x0000 0022 | SW_RESET | SW_RESET | | | | | | | | — | | | | | | | |
| p. 56 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

## 6.2 CONFIG

| Address | Register | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x0000 0040 | CLK_CFG | — | | | SYSCLK_SRC | — | | | | | | | | | | | |
| p. 56 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0000 0042 | SAMPLE_RATE | — | | | | | | | | | | | | | SAMPLE_RATE | | |
| p. 56 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0x0000 0044 | CHIP_ENABLE | — | | | | | | | | | | | | | | | GLOBAL_EN |
| p. 56 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0000 0048 | ASP_CFG | — | | | | | | | | | ASP_BCLK_INV | ASP_PRIMARY | — | | | ASP_BCLK_FREQ | |
| p. 57 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0000 0050 | SIGNAL_PATH_CFG | — | | | | | | | | | ASP_FSYNC_TYPE | ASP_TDM_SLOT | | | ASP_FORMAT | | |
| p. 57 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |



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## 6.3 INPUT_PATH

| Address | Register | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x0000 0080 | IN_ENABLES | — | | | | | | | | | | | | | | IN2_ ADC_EN | IN1_ ADC_EN |
| p. 57 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0000 0082 | IN_RAMP_SUM | — | | | | IN_CLIP_THRESH | | | | — | IN_RAMP_RATE_DEC | | | — | IN_RAMP_RATE_INC | | |
| p. 58 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| 0x0000 0086 | IN_FILTER | — | | | IN_HPF_ EN | — | | IN_FILTER_SEL | | — | | | | | | | |
| p. 58 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0000 008A | IN_INV | — | | | | | | | | | | | | | | IN2_INV | IN1_INV |
| p. 59 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0000 0090 | IN1_VOL_CTRL | IN1_ MUTE | — | | | | | | IN1_VOL | | | | | | | | |
| p. 59 | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0000 0092 | IN2_VOL_CTRL | IN2_ MUTE | — | | | | | | IN2_VOL | | | | | | | | |
| p. 59 | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0000 00A0 | IN_VOL_ UPDATE | — | | | | | | | | | | | | | | | IN_VU |
| p. 59 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

## 6.4 HGC

| Address | Register | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x0000 2000 | HGC_ CONTROL | — | | | | | | | | | | | HGC_ ABORT | — | | | HGC_ INIT_ UPDATE |
| p. 60 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0000 2004 | HGC_STATUS | — | | | | | | | | | | | | | | | HGC_ BUSY_ STS |
| p. 60 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0000 200C | IO_CTRL | — | | | | | DB_TIME | | | — | | SW_ TYPE | — | | | | HGC_ CTRL_ INTERFA CE |
| p. 60 | | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 0x0000 2010 | GPIO_STS | — | | | | GPO_STS | | | | — | | | | GPI_STS | | | |
| p. 61 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0000 2020 | SPI_CLK | — | | | | | | | | HGC_SCK_DIV | | | | — | | HGC_ CLK_PHA | HGC_ CLK_POL |
| p. 61 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0000 2022 | SPI_CSB | — | | | | HGC_CSB_IDLE_DUR | | | | HGC_CSB_RISE_DLY | | | | HGC_CSB_FALL_DLY | | | |
| p. 61 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0000 2100 | IN_CFG | — | | | | | | | | | | | IN_ STEP_ RAMP_ EN | IN_ZC_TIMEOUT | | | |
| p. 62 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 0x0000 2104 | IN_PATH_DLY_ DIG | IN_TM_DLY | | | | | | | | IN_INT_DIG_GAIN_DLY | | | | | | | |
| p. 62 | | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0x0000 2106 | IN_PATH_DLY_ ANA | — | | | | | | | | IN_INT_ANA_GAIN_DLY | | | | | | | |
| p. 63 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |


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| Address | Register | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x0000 2108 | IN_TM_CFG | IN_TM_HOLD_TIME | | | | | | | | — | | | | | | | IN_TM_EN |
| p. 63 | | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0000 2110 | IN_EMA_EN | — | | | IN_EMA_TIME | | | | | — | | | | | | IN2_EMA_EN | IN1_EMA_EN |
| p. 63 | | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0000 2114 | IN1_TM_THR | — | | | | | | | | | | | IN1_TM_LD_THR | | | | |
| p. 64 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0x0000 2118 | IN2_TM_THR | — | | | | | | | | | | | IN2_TM_LD_THR | | | | |
| p. 64 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0x0000 2140 | IN_PAD_CFG | — | | | | | | IN2_PAD_LD_EN | IN1_PAD_LD_EN | — | | | | | | IN2_PAD_AUTO_EN | IN1_PAD_AUTO_EN |
| p. 64 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0000 2142 | IN_PAD_SIGNAL | IN_PAD_LD_AVG | — | | | | | | | | | | IN_PAD_LD_TIME | | | | |
| p. 65 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| 0x0000 2146 | IN1_PAD_THR | — | | | | IN1_PAD_LOW_THR | | | | — | | | IN1_PAD_HIGH_THR | | | | |
| p. 65 | | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0x0000 214A | IN2_PAD_THR | — | | | | IN2_PAD_LOW_THR | | | | — | | | IN2_PAD_HIGH_THR | | | | |
| p. 65 | | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0x0000 2170 | IN_SIG_ACT_EN | — | | | | | | | | | | | | | | IN_SIG_ACT_EN | |
| p. 66 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0000 2176 | IN1_SIG_ACT_THR | — | | | | IN1_SIG_ACT_HIGH_THR | | | | — | | | | IN1_SIG_ACT_LOW_THR | | | |
| p. 66 | | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 0x0000 217A | IN2_SIG_ACT_THR | — | | | | IN2_SIG_ACT_HIGH_THR | | | | — | | | | IN2_SIG_ACT_LOW_THR | | | |
| p. 66 | | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 0x0000 2200 | IN1_CFG_SPI | — | | | | | IN1_SPI_POSITION | | | — | | IN1_BIT_PATT_LENGTH | | | | | |
| p. 66 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0000 2202 | IN1_CFG_GPIO | — | | | IN1_GPI_POL | — | IN1_GPI_SEL | | | — | | | | IN1_GPO4_SEL | IN1_GPO3_SEL | IN1_GPO2_SEL | IN1_GPO1_SEL |
| p. 67 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0000 2204 | IN2_CFG_SPI | — | | | | | IN2_SPI_POSITION | | | — | | IN2_BIT_PATT_LENGTH | | | | | |
| p. 67 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0000 2206 | IN2_CFG_GPIO | — | | | IN2_GPI_POL | — | IN2_GPI_SEL | | | — | | | | IN2_GPO4_SEL | IN2_GPO3_SEL | IN2_GPO2_SEL | IN2_GPO1_SEL |
| p. 67 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0000 2220 | IN1_BIT_PATT_0 | IN1_BIT_PATT_0 | | | | | | | | | | | | | | | |
| p. 68 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0000 2222 | IN1_BIT_PATT_1 | IN1_BIT_PATT_1 | | | | | | | | | | | | | | | |
| p. 68 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0000 2224 | IN1_EXT_GAIN | — | | | | | IN1_EXT_ANA_GAIN | | | | | | | | | | |
| p. 68 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0000 2226 | IN1_INT_GAIN | IN1_UPDATE | — | IN1_INT_ANA_GAIN | | | — | | IN1_INT_DIG_GAIN | | | | | | | | |
| p. 69 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0000 2228 | IN2_BIT_PATT_0 | IN2_BIT_PATT_0 | | | | | | | | | | | | | | | |
| p. 69 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0000 222A | IN2_BIT_PATT_1 | IN2_BIT_PATT_1 | | | | | | | | | | | | | | | |
| p. 69 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |


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| Address | Register | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x0000 222C | IN2_EXT_GAIN | — | | | | | IN2_EXT_ANA_GAIN | | | | | | | | | | |
| p. 69 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0000 222E | IN2_INT_GAIN | IN2_UPDATE | — | IN2_INT_ANA_GAIN | | | — | | IN2_INT_DIG_GAIN | | | | | | | | |
| p. 70 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0000 2260 | IN1_LOW_BIT_PATT_0 | IN1_LOW_BIT_PATT_0 | | | | | | | | | | | | | | | |
| p. 70 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0000 2262 | IN1_LOW_BIT_PATT_1 | IN1_LOW_BIT_PATT_1 | | | | | | | | | | | | | | | |
| p. 70 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0000 2264 | IN1_LOW_EXT_GAIN | — | | | | | IN1_LOW_EXT_ANA_GAIN | | | | | | | | | | |
| p. 70 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0000 2266 | IN1_LOW_INT_GAIN | IN1_LOW_UPDATE | — | IN1_LOW_INT_ANA_GAIN | | | — | | IN1_LOW_INT_DIG_GAIN | | | | | | | | |
| p. 71 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0000 2268 | IN2_LOW_BIT_PATT_0 | IN2_LOW_BIT_PATT_0 | | | | | | | | | | | | | | | |
| p. 71 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0000 226A | IN2_LOW_BIT_PATT_1 | IN2_LOW_BIT_PATT_1 | | | | | | | | | | | | | | | |
| p. 71 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0000 226C | IN2_LOW_EXT_GAIN | — | | | | | IN2_LOW_EXT_ANA_GAIN | | | | | | | | | | |
| p. 71 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0000 226E | IN2_LOW_INT_GAIN | IN2_LOW_UPDATE | — | IN2_LOW_INT_ANA_GAIN | | | — | | IN2_LOW_INT_DIG_GAIN | | | | | | | | |
| p. 72 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0000 22C0 | IN1_HIGH_BIT_PATT_0 | IN1_HIGH_BIT_PATT_0 | | | | | | | | | | | | | | | |
| p. 72 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0000 22C2 | IN1_HIGH_BIT_PATT_1 | IN1_HIGH_BIT_PATT_1 | | | | | | | | | | | | | | | |
| p. 72 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0000 22C4 | IN1_HIGH_EXT_GAIN | — | | | | | IN1_HIGH_EXT_ANA_GAIN | | | | | | | | | | |
| p. 72 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0000 22C6 | IN1_HIGH_INT_GAIN | IN1_HIGH_UPDATE | — | IN1_HIGH_INT_ANA_GAIN | | | — | | IN1_HIGH_INT_DIG_GAIN | | | | | | | | |
| p. 73 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0000 22C8 | IN2_HIGH_BIT_PATT_0 | IN2_HIGH_BIT_PATT_0 | | | | | | | | | | | | | | | |
| p. 73 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0000 22CA | IN2_HIGH_BIT_PATT_1 | IN2_HIGH_BIT_PATT_1 | | | | | | | | | | | | | | | |
| p. 73 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0000 22CC | IN2_HIGH_EXT_GAIN | — | | | | | IN2_HIGH_EXT_ANA_GAIN | | | | | | | | | | |
| p. 73 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0000 22CE | IN2_HIGH_INT_GAIN | IN2_HIGH_UPDATE | — | IN2_HIGH_INT_ANA_GAIN | | | — | | IN2_HIGH_INT_DIG_GAIN | | | | | | | | |
| p. 74 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0000 2900 | AUX1_CFG | — | | | | | AUX1_SPI_POSITION | | | — | | AUX1_BIT_PATT_LENGTH | | | | | |
| p. 74 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0000 2904 | AUX2_CFG | — | | | | | AUX2_SPI_POSITION | | | — | | AUX2_BIT_PATT_LENGTH | | | | | |
| p. 74 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0000 2920 | AUX1_BIT_PATT_0 | AUX1_BIT_PATT_0 | | | | | | | | | | | | | | | |
| p. 75 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0000 2922 | AUX1_BIT_PATT_1 | AUX1_BIT_PATT_1 | | | | | | | | | | | | | | | |
| p. 75 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |


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| Address | Register | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x0000 2924 | AUX2_BIT_PATT_0 | AUX2_BIT_PATT_0 | | | | | | | | | | | | | | | |
| p. 75 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0000 2926 | AUX2_BIT_PATT_1 | AUX2_BIT_PATT_1 | | | | | | | | | | | | | | | |
| p. 75 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

## 6.5 PIN_CONFIG

| Address | Register | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x0000 3D1C | PAD_IRQ_CFG | IRQ_OP_CFG | — | | | | | | GPIO1_IRQ_EN | GPIO2_IRQ_EN | — | | CONFIG4_IRQ_EN | SPI_SCK_IRQ_EN | — | | |
| p. 75 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

## 6.6 IRQ_CONFIG

| Address | Register | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0x0000 3E04 | IRQ_STS | — | | | | | | | | | | | | | | | IRQ_STS |
| p. 76 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0000 3E1C | IRQ_ADC_EVENT_INT | — | | | | IN2_PAD_LOW_INT | IN1_PAD_LOW_INT | IN2_PAD_HIGH_INT | IN1_PAD_HIGH_INT | GAIN_CONFLICT_INT | — | | | | IN2_CLIP_WARN_INT | IN1_CLIP_WARN_INT | — |
| p. 76 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0000 3E1E | IRQ_HGC_EVENT_INT | — | | | | | | | | | | | HGC_SPI_ERROR_INT | HGC_ABORT_ERROR_INT | — | HGC_ERROR_INT | HGC_DONE_INT |
| p. 77 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0000 3E2C | IRQ_ADC_EVENT_MASK | — | | | | IN2_PAD_LOW_MASK | IN1_PAD_LOW_MASK | IN2_PAD_HIGH_MASK | IN1_PAD_HIGH_MASK | GAIN_CONFLICT_MASK | — | | | | IN2_CLIP_WARN_MASK | IN1_CLIP_WARN_MASK | — |
| p. 77 | | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0x0000 3E2E | IRQ_HGC_EVENT_MASK | — | | | | | | | | | | | HGC_SPI_ERROR_MASK | HGC_ABORT_MASK | — | HGC_ERROR_MASK | HGC_DONE_MASK |
| p. 78 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| 0x0000 3E5C | IRQ_ADC_EVENT_STS | — | | | | IN2_PAD_LOW_STS | IN1_PAD_LOW_STS | IN2_PAD_HIGH_STS | IN1_PAD_HIGH_STS | — | | | | | IN2_CLIP_WARN_STS | IN1_CLIP_WARN_STS | — |
| p. 78 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |


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# 7 Register Descriptions

This section describes each of the control port registers.

This register view is for the CS5312S.

- The register field default values are established upon the deassertion of the $\overline{\text{RESET}}$ pin or following soft reset.
- A "—" represents a reserved field/access type.
- The reserved field values must not be modified.
- The registers are 16 bits wide, and only word transactions are allowed.
- All visible fields are read/write except where indicated with the following shading:

Read/write access  Read-only access  Write-only access

## 7.1 DEVID

### 7.1.1 DEVID_0

**Address: 0x0000 0000**

| RO | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DEVID_0 | | | | | | | | | | | | | | | |
| Default | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |

| Bits | Name | Description |
|---|---|---|
| 15:0 | DEVID_0 | This register indicates the lower bytes of Device ID CS5312S<br>0x0000–0x3122 = Reserved<br>0x3123 = (Default) CS5312S<br>0x3124–0xFFFF = Reserved |

### 7.1.2 DEVID_1

**Address: 0x0000 0002**

| RO | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | DEVID_1 | | | | | | | | | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

| Bits | Name | Description |
|---|---|---|
| 15:0 | DEVID_1 | This register indicates the upper bytes of Device ID CS5312S<br>0x0000–0x0004 = Reserved<br>0x0005 = (Default) CS5312S<br>0x0006–0xFFFF = Reserved |

### 7.1.3 REVID

**Address: 0x0000 0004**

| RO | 15…8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| | — | AREVID | | | | MTLREVID | | | |
| Default | 0x00 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |

| Bits | Name | Description |
|---|---|---|
| 15:8 | — | Reserved |
| 7:4 | AREVID | This field indicates the all-layer device revision.<br>0x0–0x9 = Reserved<br>0xA = (Default) Revision Ax<br>0xB–0xF = Reserved |
| 3:0 | MTLREVID | This field indicates the metal-layer device revision.<br>0x0 = Reserved<br>0x1 = (Default) Revision x1<br>0x2–0xF = Reserved |


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### 7.1.4 SW_RESET

**Address: 0x0000 0022**

| WO | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | SW_RESET | | | | | | | | — | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15:8 | SW_RESET | Software Reset. Writing 0x5A triggers a reset.<br>0x00 = (Default) No action<br>0x01–0x59 = Reserved<br>0x5A = Software reset<br>0x5B–0xFF = Reserved |
| 7:0 | — | Reserved |

## 7.2 CONFIG

### 7.2.1 CLK_CFG

**Address: 0x0000 0040**

| RW | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | — | | | SYSCLK_SRC | — | | | | | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15:13 | — | Reserved |
| 12 | SYSCLK_SRC | System clock source. If XTAL is selected, the MCLK is the output clock.<br>0 = (Default) MCLK input<br>1 = XTAL input |
| 11:0 | — | Reserved |

### 7.2.2 SAMPLE_RATE

**Address: 0x0000 0042**

| RW | 15…8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| | — | — | | | | | SAMPLE_RATE | | |
| Default | 0x00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

| Bits | Name | Description |
|---|---|---|
| 15:3 | — | Reserved |
| 2:0 | SAMPLE_RATE | Audio sample frequency. Note the sample rate must be integer-related to the system clock frequency. Auto-detect is only valid if sample rate = 16-192 kHz, and the ASP is in Secondary Mode.<br>000 = 32 kHz<br>001 = (Default) 48/44.1 kHz<br>010 = 96/88.2 kHz<br>011 = 192/176.4 kHz<br>100 = 384/352.8 kHz<br>101 = Reserved<br>110 = Auto-detect<br>111 = 16 kHz |

### 7.2.3 CHIP_ENABLE

**Address: 0x0000 0044**

| RW | 15…8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| | — | — | | | | | | | GLOBAL_EN |
| Default | 0x00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15:1 | — | Reserved |
| 0 | GLOBAL_EN | Global enable. Set to 1 to configure and enable all functions. Clear to 0 to disable. Note the clocking and ASP control registers are only valid on the rising edge of GLOBAL_EN. It is recommended to select the disabled state (GLOBAL_EN=0) before writing to these registers. |


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### 7.2.4 ASP_CFG

**Address: 0x0000 0048**

| RW | 15…8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| | — | — | ASP_BCLK_INV | ASP_PRIMARY | — | | | ASP_BCLK_FREQ | |
| Default | 0x00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15:7 | — | Reserved |
| 6 | ASP_BCLK_INV | ASP BCLK polarity. Selects the valid BCLK edge for data sampling.<br>In non-inverted mode, DOUT data is driven on BCLK falling edge (TDM half-cycle mode) or rising edge (TDM full-cycle mode).<br>In inverted mode, DOUT data is driven on BCLK rising edge (TDM half-cycle mode) or falling edge (TDM full-cycle mode).<br>0 = (Default) Non-inverted<br>1 = Inverted |
| 5 | ASP_PRIMARY | ASP Primary/Secondary Mode select. In ASP Primary Mode, BCLK and FSYNC are outputs. In ASP Secondary Mode, BCLK and FSYNC are inputs.<br>0 = (Default) Secondary Mode<br>1 = Primary Mode |
| 4:2 | — | Reserved |
| 1:0 | ASP_BCLK_FREQ | ASP BCLK frequency. The BCLK frequency must be high enough to support the required number of data bits at the selected sample rate. Only valid in ASP Primary Mode.<br>Note the BCLK frequency is integer-related to the system clock frequency i.e., multiples of 3.072 MHz for 24.576 MHz system clock, or multiples of 2.8224 MHz for 22.5792 MHz system clock.<br>00 = (Default) 3.072/2.8224 MHz<br>01 = 6.144/5.6448 MHz<br>10 = 12.288/11.2896 MHz<br>11 = 24.576/22.5792 MHz |

### 7.2.5 SIGNAL_PATH_CFG

**Address: 0x0000 0050**

| RW | 15…8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| | — | — | ASP_FSYNC_TYPE | ASP_TDM_SLOT | | | ASP_FORMAT | | |
| Default | 0x00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15:7 | — | Reserved |
| 6 | ASP_FSYNC_TYPE | Configure ASP_FSYNC as pulse or square wave (50% duty cycle) in TDM mode. Only applicable when ASP is in Primary Mode.<br>0 = (Default) FSYNC Pulse<br>1 = FSYNC Square Wave |
| 5:3 | ASP_TDM_SLOT | TDM slot select. Configures which TDM slots are used in TDM maximum-time-slots mode.<br>000 = (Default) Slots 0-1<br>001 = Slots 2-3<br>010 = Slots 4-5<br>011 = Slots 6-7<br>100 = Slots 8-9<br>101 = Slots 10-11<br>110 = Slots 12-13<br>111 = Slots 14-15 |
| 2:0 | ASP_FORMAT | ASP data format. Selects how the audio samples are arranged within the FSYNC frame.<br>000 = (Default) I2S Mode<br>001 = Left-Justified Mode<br>010–100 = Reserved<br>101 = TDM Mode maximum time slots, full cycle<br>110 = TDM Mode maximum time slots, half cycle<br>111 = TDM Mode minimum time slots |

## 7.3 INPUT_PATH

### 7.3.1 IN_ENABLES

**Address: 0x0000 0080**

| RW | 15…8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| | — | — | | | | | | IN2_ADC_EN | IN1_ADC_EN |
| Default | 0x00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15:2 | — | Reserved |


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| Bits | Name | Description |
|---|---|---|
| 1 | IN2_ADC_EN | Channel 2 input enable. Note that Channels 1-2 should always be enabled/disabled as a pair.<br>0 = (Default) Disabled<br>1 = Enabled |
| 0 | IN1_ADC_EN | Channel 1 input enable. Note that Channels 1-2 should always be enabled/disabled as a pair.<br>0 = (Default) Disabled<br>1 = Enabled |

## 7.3.2 IN_RAMP_SUM

**Address: 0x0000 0082**

| RW | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | — | | | | IN_CLIP_THRESH | | | | — | IN_RAMP_RATE_DEC | | | — | IN_RAMP_RATE_INC | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15:12 | — | Reserved |
| 11:8 | IN_CLIP_THRESH | Input clip-warning threshold.<br>0x0 = (Default) 0.0 dBFS<br>0x1 = –0.125 dBFS<br>0x2 = –0.25 dBFS<br>0x3 = –0.5 dBFS<br>0x4 = –1.0 dBFS<br>0x5 = –3.0 dBFS<br>0x6 = –6.0 dBFS<br>0x7–0xF = Reserved |
| 7 | — | Reserved |
| 6:4 | IN_RAMP_RATE_DEC | ADC input volume Decrease Ramp Rate (ms/6 dB), used for gain changes. This field should not be changed while a volume ramp is in progress.<br>000 = 0 ms<br>001 = 0.5 ms<br>010 = (Default) 1 ms<br>011 = 2 ms<br>100 = 4 ms<br>101 = 8 ms<br>110 = 15 ms<br>111 = 30 ms |
| 3 | — | Reserved |
| 2:0 | IN_RAMP_RATE_INC | ADC input volume Increase Ramp Rate (ms/6 dB), used for gain changes. This field should not be changed while a volume ramp is in progress.<br>000 = 0 ms<br>001 = 0.5 ms<br>010 = (Default) 1 ms<br>011 = 2 ms<br>100 = 4 ms<br>101 = 8 ms<br>110 = 15 ms<br>111 = 30 ms |

## 7.3.3 IN_FILTER

**Address: 0x0000 0086**

| RW | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | — | | | IN_HPF_EN | — | | IN_FILTER_SEL | | — | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15:13 | — | Reserved |
| 12 | IN_HPF_EN | High-pass filter enable.<br>0 = (Default) HPF disabled<br>1 = HPF enabled |
| 11:10 | — | Reserved |
| 9:8 | IN_FILTER_SEL | Digital filter select. Configures the decimation filter.<br>00 = (Default) Minimum phase, Slow roll-off<br>01 = Minimum phase, Fast roll-off<br>10 = Linear phase, Slow roll-off<br>11 = Linear phase, Fast roll-off |
| 7:0 | — | Reserved |


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### 7.3.4 IN_INV

**Address: 0x0000 008A**

| RW | 15…8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| | — | — | | | | | | IN2_INV | IN1_INV |
| Default | 0x00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15:2 | — | Reserved |
| 1 | IN2_INV | Channel 2 ADC invert.<br>0 = (Default) No inversion<br>1 = ADC data invert |
| 0 | IN1_INV | Channel 1 ADC invert.<br>0 = (Default) No inversion<br>1 = ADC data invert |

### 7.3.5 IN1_VOL_CTRL

**Address: 0x0000 0090**

| RW | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | IN1_MUTE | — | | | | | | | IN1_VOL | | | | | | | |
| Default | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15 | IN1_MUTE | Channel 1 input mute.<br>0 = Unmute<br>1 = (Default) Mute |
| 14:9 | — | Reserved |
| 8:0 | IN1_VOL | Channel 1 input digital volume, –127.5 dB to +30 dB in 0.5 dB steps.<br>0x000 = (Default) 0.0 dB<br>0x001 = –0.5 dB<br>…<br>0x0FF = –127.5 dB<br>0x100 = Reserved<br>0x101 = 0.5 dB<br>0x102 = 1.0 dB<br>…<br>0x13C = 30.0 dB<br>0x13D–0x1FF = Reserved |

### 7.3.6 IN2_VOL_CTRL

**Address: 0x0000 0092**

| RW | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | IN2_MUTE | — | | | | | | | IN2_VOL | | | | | | | |
| Default | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15 | IN2_MUTE | Channel 2 input mute.<br>0 = Unmute<br>1 = (Default) Mute |
| 14:9 | — | Reserved |
| 8:0 | IN2_VOL | Channel 2 input digital volume, –127.5 dB to +30 dB in 0.5 dB steps.<br>0x000 = (Default) 0.0 dB<br>0x001 = –0.5 dB<br>…<br>0x0FF = –127.5 dB<br>0x100 = Reserved<br>0x101 = 0.5 dB<br>0x102 = 1.0 dB<br>…<br>0x13C = 30.0 dB<br>0x13D–0x1FF = Reserved |

### 7.3.7 IN_VOL_UPDATE

**Address: 0x0000 00A0**

| WO | 15…8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| | — | — | | | | | | | IN_VU |
| Default | 0x00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15:1 | — | Reserved |
| 0 | IN_VU | Global ADC input volume update trigger.<br>0 = (Default) No action<br>1 = Write 1 to trigger an update of all input volume/mute registers |


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# 7.4 HGC

## 7.4.1 HGC_CONTROL

**Address: 0x0000 2000**

| WO | 15…8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| | — | — | | | HGC_ABORT | — | | | HGC_INIT_UPDATE |
| Default | 0x00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15:5 | — | Reserved |
| 4 | HGC_ABORT | Abort gain updates. Write 1 to abort any pending gain updates. Note that any updates already in progress will complete as normal and are not aborted.<br>0 = (Default) No action<br>1 = Write 1 to abort gain updates |
| 3:1 | — | Reserved |
| 0 | HGC_INIT_UPDATE | Initialize gain settings. Write 1 to transmit the SPI bit patterns and initialize all gain settings. Note the zero-cross detection is not applied when initializing gain settings.<br>0 = (Default) No action<br>1 = Write 1 to initialize gain settings |

## 7.4.2 HGC_STATUS

**Address: 0x0000 2004**

| RO | 15…8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| | — | — | | | | | | | HGC_BUSY_STS |
| Default | 0x00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15:1 | — | Reserved |
| 0 | HGC_BUSY_STS | Busy status. Indicates gain updates are pending for one or more audio channels.<br>0 = (Default) Idle<br>1 = Busy |

## 7.4.3 IO_CTRL

**Address: 0x0000 200C**

| RW | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | — | | | | | DB_TIME | | | — | | SW_TYPE | — | | | | HGC_CTRL_INTERFACE |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |

| Bits | Name | Description |
|---|---|---|
| 15:11 | — | Reserved |
| 10:8 | DB_TIME | GPI debounce time, base 32 kHz.<br>000 = 124 us<br>001 = 2 ms<br>010 = 4 ms<br>011 = (Default) 8 ms<br>100 = 16 ms<br>101 = 32 ms<br>110 = 64 ms<br>111 = 128 ms |
| 7:6 | — | Reserved |
| 5 | SW_TYPE | GPI type selection. Select toggle switch for rising-edge detection or latching switch for level detection.<br>0 = Toggle switch<br>1 = (Default) Latching switch |
| 4:1 | — | Reserved |
| 0 | HGC_CTRL_INTERFACE | Selects GPO/HGC_SPI control interface.<br>0 = HGC using SPI<br>1 = (Default) HGC using GPO |


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### 7.4.4 GPIO_STS

**Address: 0x0000 2010**

| RO | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | — | | | | GPO_STS | | | | — | | | | GPI_STS | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15:12 | — | Reserved |
| 11:8 | GPO_STS | GPO read back status. |
| 7:4 | — | Reserved |
| 3:0 | GPI_STS | GPI read back status. |

### 7.4.5 SPI_CLK

**Address: 0x0000 2020**

| RW | 15…8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| | — | HGC_SCK_DIV | | | | — | | HGC_CLK_PHA | HGC_CLK_POL |
| Default | 0x00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15:8 | — | Reserved |
| 7:4 | HGC_SCK_DIV | SPI clock divider. Configures the SPI clock frequency as a division of the system clock.<br>For 48 kHz-related sample rates, the SPI clock is a division of system clock (24.576 MHz). For 44.1 kHz-related sample rates, the SPI clock is a division of system clock (22.5792 MHz).<br>0x0 = (Default) Divide by 2<br>0x1 = Divide by 4<br>0x2 = Divide by 6<br>0x3 = Divide by 8<br>0x4 = Divide by 10<br>0x5 = Divide by 12<br>0x6 = Divide by 14<br>0x7 = Divide by 16<br>0x8 = Divide by 18<br>0x9 = Divide by 20<br>0xA = Divide by 22<br>0xB = Divide by 24<br>0xC = Divide by 26<br>0xD = Divide by 28<br>0xE = Divide by 30<br>0xF = Divide by 32 |
| 3:2 | — | Reserved |
| 1 | HGC_CLK_PHA | SPI clock phase select.<br>0 = (Default) Negative SPI clock phase<br>1 = Positive SPI clock phase |
| 0 | HGC_CLK_POL | SPI clock polarity select.<br>0 = (Default) Negative SPI clock polarity<br>1 = Positive SPI clock polarity |

### 7.4.6 SPI_CSB

**Address: 0x0000 2022**

| RW | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | — | | | | HGC_CSB_IDLE_DUR | | | | HGC_CSB_RISE_DLY | | | | HGC_CSB_FALL_DLY | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15:12 | — | Reserved |
| 11:8 | HGC_CSB_IDLE_DUR | Minimum idle duration between SPI transactions (from CS rising edge to CS falling edge). The duration is defined in system-clock cycles.<br>For 48 kHz-related sample rates, the system-clock period is 1/24.576 MHz. For 44.1 kHz-related sample rates, the system-clock period is 1/22.5792 MHz.<br>0x0 = (Default) 32 clock cycles<br>0x1 = 36 clock cycles<br>0x2 = 40 clock cycles<br>0x3 = 44 clock cycles<br>0x4 = 48 clock cycles<br>0x5 = 56 clock cycles<br>0x6 = 64 clock cycles<br>0x7 = 80 clock cycles<br>0x8 = 96 clock cycles<br>0x9 = 128 clock cycles<br>0xA = 160 clock cycles<br>0xB = 224 clock cycles<br>0xC = 288 clock cycles<br>0xD = 416 clock cycles<br>0xE = 544 clock cycles<br>0xF = 800 clock cycles |


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| Bits | Name | Description |
|---|---|---|
| 7:4 | HGC_CSB_RISE_DLY | Chip Select (CS) rise delay. Configures the minimum time from SCLK active edge to CS rising edge (end of SPI transaction). The delay is defined in system-clock cycles.<br>For 48 kHz-related sample rates, the system-clock period is 1/24.576 MHz. For 44.1 kHz-related sample rates, the system-clock period is 1/22.5792 MHz.<br>0x0 = (Default) 4 clock cycles<br>0x1 = 6 clock cycles<br>0x2 = 8 clock cycles<br>0x3 = 10 clock cycles<br>0x4 = 12 clock cycles<br>0x5 = 14 clock cycles<br>0x6 = 16 clock cycles<br>0x7 = 18 clock cycles<br>0x8 = 20 clock cycles<br>0x9 = 22 clock cycles<br>0xA = 24 clock cycles<br>0xB = 26 clock cycles<br>0xC = 28 clock cycles<br>0xD = 30 clock cycles<br>0xE = 32 clock cycles<br>0xF = 34 clock cycles |
| 3:0 | HGC_CSB_FALL_DLY | Chip Select (CS) fall delay. Configures the minimum time from CS falling edge to SCLK active edge (start of SPI transaction). The delay is defined in system-clock cycles.<br>For 48 kHz-related sample rates, the system-clock period is 1/24.576 MHz. For 44.1 kHz-related sample rates, the system-clock period is 1/22.5792 MHz.<br>The delay is dependent on the SPI clock divider (SCK_DIV) setting – the 'N' variable in the enumeration represents the value of HGC_SCK_DIV field (0-15).<br>0x0 = (Default) 4+N clock cycles<br>0x1 = 6+N clock cycles<br>0x2 = 8+N clock cycles<br>0x3 = 10+N clock cycles<br>0x4 = 12+N clock cycles<br>0x5 = 14+N clock cycles<br>0x6 = 16+N clock cycles<br>0x7 = 18+N clock cycles<br>0x8 = 20+N clock cycles<br>0x9 = 22+N clock cycles<br>0xA = 24+N clock cycles<br>0xB = 26+N clock cycles<br>0xC = 28+N clock cycles<br>0xD = 30+N clock cycles<br>0xE = 32+N clock cycles<br>0xF = 34+N clock cycles |

## 7.4.7 IN_CFG

**Address: 0x0000 2100**

| RW | 15…8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| | — | — | | | IN_STEP_RAMP_EN | IN_ZC_TIMEOUT | | | |
| Default | 0x00 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |

| Bits | Name | Description |
|---|---|---|
| 15:5 | — | Reserved |
| 4 | IN_STEP_RAMP_EN | Step ramp enable. Enables the digital gain to be used to compensate for step changes in the analog gain.<br>0 = (Default) Disabled<br>1 = Enabled |
| 3:0 | IN_ZC_TIMEOUT | Timeout for zero-cross detection.<br>0x0 = 0 (OFF)<br>0x1–0x2 = Reserved<br>0x3 = 1 ms<br>0x4 = 2 ms<br>0x5 = 5 ms<br>0x6 = 10 ms<br>0x7 = (Default) 20 ms<br>0x8 = 50 ms<br>0x9 = 100 ms<br>0xA–0xF = Reserved |

## 7.4.8 IN_PATH_DLY_DIG

**Address: 0x0000 2104**

| RW | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | IN_TM_DLY | | | | | | | | IN_INT_DIG_GAIN_DLY | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15:8 | IN_TM_DLY | Transient masking delay. Configures the delay from the external analog-gain update to the start of the transient-masking period. The delay is defined in audio sample (1/fs) units.<br>0x00 = 0 samples<br>0x01 = 1 samples<br>…<br>0x03 = (Default) 3 samples<br>…<br>0xFF = 255 samples |
| 7:0 | IN_INT_DIG_GAIN_DLY | Digital gain update delay. Configures the delay from the internal analog-gain update to the digital-gain update. The delay is defined in audio sample (1/fs) units.<br>0x00 = 0 samples<br>0x01 = 1 samples<br>…<br>0x04 = (Default) 4 samples<br>…<br>0xFF = 255 samples |


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### 7.4.9 IN_PATH_DLY_ANA

**Address: 0x0000 2106**

| RW | 15…8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| | — | IN_INT_ANA_GAIN_DLY | | | | | | | |
| Default | 0x00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15:8 | — | Reserved |
| 7:0 | IN_INT_ANA_GAIN_DLY | Internal analog gain update delay. Configures the delay from the external analog gain update to the internal analog gain update. The delay is defined in system-clock cycles.<br>For 48 kHz-related sample rates, the system-clock period is 1/24.576 MHz. For 44.1 kHz-related sample rates, the system-clock period is 1/22.5792 MHz.<br>0x00 = (Default) 0 clock cycles<br>0x01 = 1 clock cycles<br>…<br>0xFF = 255 clock cycles |

### 7.4.10 IN_TM_CFG

**Address: 0x0000 2108**

| RW | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | IN_TM_HOLD_TIME | | | | | | | | — | | | | | | | IN_TM_EN |
| Default | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15:8 | IN_TM_HOLD_TIME | Transient masking hold time. Configures the duration of the transient masking. The delay is defined in audio sample (1/fs) units.<br>0x00 = 0 samples<br>0x01 = 1 samples<br>…<br>0x07 = (Default) 7 samples<br>…<br>0xFF = 255 samples |
| 7:1 | — | Reserved |
| 0 | IN_TM_EN | Transient masking enable.<br>0 = (Default) Disabled<br>1 = Enabled |

### 7.4.11 IN_EMA_EN

**Address: 0x0000 2110**

| RW | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | — | | | IN_EMA_TIME | | | | | — | | | | | | IN2_EMA_EN | IN1_EMA_EN |
| Default | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15:13 | — | Reserved |
| 12:8 | IN_EMA_TIME | EMA filter time constant. The time constant is defined in audio sample (1/fs) units.<br>0x00–0x09 = Reserved<br>0x0A = 1024 samples<br>0x0B = 2048 samples<br>0x0C = (Default) 4096 samples<br>0x0D = 8192 samples<br>0x0E = 16384 samples<br>0x0F = 32768 samples<br>0x10 = 65536 samples<br>0x11–0x1F = Reserved |
| 7:2 | — | Reserved |
| 1 | IN2_EMA_EN | Input Channel 2 EMA filter enable.<br>0 = (Default) Disabled<br>1 = Enabled |
| 0 | IN1_EMA_EN | Input Channel 1 EMA filter enable.<br>0 = (Default) Disabled<br>1 = Enabled |


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### 7.4.12 IN1_TM_THR

**Address: 0x0000 2114**

| RW | 15…8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| | — | — | | | IN1_TM_LD_THR | | | | |
| Default | 0x00 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |

| Bits | Name | Description |
|---|---|---|
| 15:5 | — | Reserved |
| 4:0 | IN1_TM_LD_THR | Input Channel 1 transient masking level-detect threshold. Transient masking is applied if the signal level is below the threshold.<br>0x00–0x02 = Reserved<br>0x03 = –2 dBFS<br>…<br>0x09 = (Default) –38 dBFS<br>…<br>0x13 = –98 dBFS<br>0x14–0x1F = Reserved |

### 7.4.13 IN2_TM_THR

**Address: 0x0000 2118**

| RW | 15…8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| | — | — | | | IN2_TM_LD_THR | | | | |
| Default | 0x00 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |

| Bits | Name | Description |
|---|---|---|
| 15:5 | — | Reserved |
| 4:0 | IN2_TM_LD_THR | Input Channel 2 transient masking level-detect threshold. Transient masking is applied if the signal level is below the threshold.<br>0x00–0x02 = Reserved<br>0x03 = –2 dBFS<br>…<br>0x09 = (Default) –38 dBFS<br>…<br>0x13 = –98 dBFS<br>0x14–0x1F = Reserved |

### 7.4.14 IN_PAD_CFG

**Address: 0x0000 2140**

| RW | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | — | | | | | | IN2_PAD_LD_EN | IN1_PAD_LD_EN | — | | | | | | IN2_PAD_AUTO_EN | IN1_PAD_AUTO_EN |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15:10 | — | Reserved |
| 9 | IN2_PAD_LD_EN | Input Channel 2 PAD level detector (LD) enable.<br>0 = (Default) Disabled<br>1 = Enabled |
| 8 | IN1_PAD_LD_EN | Input Channel 1 PAD level detector (LD) enable.<br>0 = (Default) Disabled<br>1 = Enabled |
| 7:2 | — | Reserved |
| 1 | IN2_PAD_AUTO_EN | Input Channel 2 PAD automatic response enable.<br>0 = (Default) Disabled<br>1 = Enabled |
| 0 | IN1_PAD_AUTO_EN | Input Channel 1 PAD automatic response enable.<br>0 = (Default) Disabled<br>1 = Enabled |


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## 7.4.15 IN_PAD_SIGNAL

**Address: 0x0000 2142**

| RW | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | IN_PAD_LD_AVG | — | | | | | | | | | | IN_PAD_LD_TIME | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15 | IN_PAD_LD_AVG | Selects averaged or instantaneous input signal for PAD high-level threshold level detection (LD).<br>0 = (Default) Averaged signal<br>1 = Instantaneous signal |
| 14:5 | — | Reserved |
| 4:0 | IN_PAD_LD_TIME | PAD level-detect time constant. The time constant is defined in audio sample (1/fs) units.<br>0x00–0x09 = Reserved<br>0x0A = 1024 samples<br>0x0B = 2048 samples<br>0x0C = (Default) 4096 samples<br>0x0D = 8192 samples<br>0x0E = 16384 samples<br>0x0F = 32768 samples<br>0x10 = 65536 samples<br>0x11–0x1F = Reserved |

## 7.4.16 IN1_PAD_THR

**Address: 0x0000 2146**

| RW | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | — | | | | IN1_PAD_LOW_THR | | | | — | | | | IN1_PAD_HIGH_THR | | | |
| Default | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |

| Bits | Name | Description |
|---|---|---|
| 15:12 | — | Reserved |
| 11:8 | IN1_PAD_LOW_THR | Input Channel 1 PAD level detector (LD) low-level threshold.<br>0x0–0x2 = Reserved<br>0x3 = –32 dBFS<br>…<br>0x9 = –68 dBFS<br>0xA = (Default) –74 dBFS<br>0xB–0xE = Reserved<br>0xF = mute |
| 7:5 | — | Reserved |
| 4:0 | IN1_PAD_HIGH_THR | Input Channel 1 PAD level detector (LD) high-level threshold. The listed threshold values apply to signal detection using the averaged signal level, the stated values represent the approximate signal levels that would be detected as above the threshold. If signal detection uses the instantaneous signal level the stated thresholds are approximately 4 dB lower, where 0x00 = –1 dBFS … (step = –1 dBFS) … 0x1F = –32 dBFS.<br>0x00–0x03 = Reserved<br>0x04 = –1 dBFS<br>…<br>0x09 = (Default) –6 dBFS<br>…<br>0x1F = –28 dBFS |

## 7.4.17 IN2_PAD_THR

**Address: 0x0000 214A**

| RW | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | — | | | | IN2_PAD_LOW_THR | | | | — | | | | IN2_PAD_HIGH_THR | | | |
| Default | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |

| Bits | Name | Description |
|---|---|---|
| 15:12 | — | Reserved |
| 11:8 | IN2_PAD_LOW_THR | Input Channel 2 PAD level detector (LD) low-level threshold.<br>0x0–0x2 = Reserved<br>0x3 = –32 dBFS<br>…<br>0x9 = –68 dBFS<br>0xA = (Default) –74 dBFS<br>0xB–0xE = Reserved<br>0xF = mute |
| 7:5 | — | Reserved |
| 4:0 | IN2_PAD_HIGH_THR | Input Channel 2 PAD level detector (LD) high-level threshold. The listed threshold values apply to signal detection using the averaged signal level, the stated values represent the approximate signal levels that would be detected as above the threshold. If signal detection uses the instantaneous signal level the stated thresholds are approximately 4 dB lower, where 0x00 = –1 dBFS … (step = –1 dBFS) … 0x1F = –32 dBFS.<br>0x00–0x03 = Reserved<br>0x04 = –1 dBFS<br>…<br>0x09 = (Default) –6 dBFS<br>…<br>0x1F = –28 dBFS |


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## 7.4.18 IN_SIG_ACT_EN

**Address: 0x0000 2170**

| RW | 15…8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| | — | — | | | | | | IN_SIG_ACT_EN | |
| Default | 0x00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15:2 | — | Reserved |
| 1:0 | IN_SIG_ACT_EN | Input signal-activity detection enable.<br>00 = (Default) Disabled<br>01–10 = Reserved<br>11 = Enabled |

## 7.4.19 IN1_SIG_ACT_THR

**Address: 0x0000 2176**

| RW | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | — | | | | IN1_SIG_ACT_HIGH_THR | | | | — | | | | IN1_SIG_ACT_LOW_THR | | | |
| Default | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |

| Bits | Name | Description |
|---|---|---|
| 15:12 | — | Reserved |
| 11:8 | IN1_SIG_ACT_ HIGH_THR | Input Channel 1 signal-activity detection, high-level threshold.<br>0x0–0x2 = Reserved<br>0x3 = –32 dBFS<br>…<br>0xA = (Default) –74 dBFS<br>0xB–0xE = Reserved<br>0xF = mute |
| 7:4 | — | Reserved |
| 3:0 | IN1_SIG_ACT_ LOW_THR | Input Channel 1 signal-activity detection, low-level threshold.<br>0x0–0x2 = Reserved<br>0x3 = –74 dBFS<br>…<br>0x7 = (Default) –98 dBFS<br>0x8–0xE = Reserved<br>0xF = mute |

## 7.4.20 IN2_SIG_ACT_THR

**Address: 0x0000 217A**

| RW | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | — | | | | IN2_SIG_ACT_HIGH_THR | | | | — | | | | IN2_SIG_ACT_LOW_THR | | | |
| Default | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |

| Bits | Name | Description |
|---|---|---|
| 15:12 | — | Reserved |
| 11:8 | IN2_SIG_ACT_ HIGH_THR | Input Channel 2 signal-activity detection high-level threshold.<br>0x0–0x2 = Reserved<br>0x3 = –32 dBFS<br>…<br>0xA = (Default) –74 dBFS<br>0xB–0xE = Reserved<br>0xF = mute |
| 7:4 | — | Reserved |
| 3:0 | IN2_SIG_ACT_ LOW_THR | Input Channel 2 signal-activity detection low-level threshold.<br>0x0–0x2 = Reserved<br>0x3 = –74 dBFS<br>…<br>0x7 = (Default) –98 dBFS<br>0x8–0xE = Reserved<br>0xF = mute |

## 7.4.21 IN1_CFG_SPI

**Address: 0x0000 2200**

| RW | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | — | | | | | IN1_SPI_POSITION | | | — | | IN1_BIT_PATT_LENGTH | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15:11 | — | Reserved |
| 10:8 | IN1_SPI_POSITION | Input Channel 1 device position in the SPI chain. |
| 7:6 | — | Reserved |
| 5:0 | IN1_BIT_PATT_ LENGTH | Input Channel 1 bit-pattern length for SPI gain control.<br>0x00 = (Default) 0 bits (device not present)<br>0x01 = 1 bits<br>0x02 = 2 bits<br>…<br>0x20 = 32 bits<br>0x21–0x3F = Reserved |



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## 7.4.22 IN1_CFG_GPIO

**Address: 0x0000 2202**

| RW | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | — | | | IN1_GPI_POL | — | IN1_GPI_SEL | | | — | | | | IN1_GPO4_SEL | IN1_GPO3_SEL | IN1_GPO2_SEL | IN1_GPO1_SEL |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15:13 | — | Reserved |
| 12 | IN1_GPI_POL | Input Channel 1 GPI polarity.<br>0 = (Default) GPI not inverted<br>1 = GPI inverted |
| 11 | — | Reserved |
| 10:8 | IN1_GPI_SEL | Select GPIO pin as GPI for input Channel 1.<br>000 = (Default) Select GPI disabled<br>001 = Select GPIO1<br>010 = Select GPIO2<br>011 = Select GPIO3<br>100 = Select GPIO4<br>101–111 = Reserved |
| 7:4 | — | Reserved |
| 3 | IN1_GPO4_SEL | Input Channel 1 GPO4 configuration.<br>0 = (Default) Disabled<br>1 = Enabled |
| 2 | IN1_GPO3_SEL | Input Channel 1 GPO3 configuration.<br>0 = (Default) Disabled<br>1 = Enabled |
| 1 | IN1_GPO2_SEL | Input Channel 1 GPO2 configuration.<br>0 = (Default) Disabled<br>1 = Enabled |
| 0 | IN1_GPO1_SEL | Input Channel 1 GPO1 configuration.<br>0 = (Default) Disabled<br>1 = Enabled |

## 7.4.23 IN2_CFG_SPI

**Address: 0x0000 2204**

| RW | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | — | | | | | IN2_SPI_POSITION | | | — | | IN2_BIT_PATT_LENGTH | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15:11 | — | Reserved |
| 10:8 | IN2_SPI_POSITION | Input Channel 2 device position in the SPI chain. |
| 7:6 | — | Reserved |
| 5:0 | IN2_BIT_PATT_LENGTH | Input Channel 2 bit-pattern length for SPI gain control.<br>0x00 = (Default) 0 bits (device not present)<br>0x01 = 1 bits<br>0x02 = 2 bits<br>…<br>0x20 = 32 bits<br>0x21–0x3F = Reserved |

## 7.4.24 IN2_CFG_GPIO

**Address: 0x0000 2206**

| RW | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | — | | | IN2_GPI_POL | — | IN2_GPI_SEL | | | — | | | | IN2_GPO4_SEL | IN2_GPO3_SEL | IN2_GPO2_SEL | IN2_GPO1_SEL |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15:13 | — | Reserved |
| 12 | IN2_GPI_POL | GPI polarity for input Channel 2.<br>0 = (Default) GPI not inverted<br>1 = GPI inverted |
| 11 | — | Reserved |


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| Bits | Name | Description |
|---|---|---|
| 10:8 | IN2_GPI_SEL | Select GPIO pin as GPI for input Channel 2.<br>000 = (Default) Select GPI disabled<br>001 = Select GPIO1<br>010 = Select GPIO2<br>011 = Select GPIO3<br>100 = Select GPIO4<br>101–111 = Reserved |
| 7:4 | — | Reserved |
| 3 | IN2_GPO4_SEL | Input Channel 2 GPO4 configuration.<br>0 = (Default) Disabled<br>1 = Enabled |
| 2 | IN2_GPO3_SEL | Input Channel 2 GPO3 configuration.<br>0 = (Default) Disabled<br>1 = Enabled |
| 1 | IN2_GPO2_SEL | Input Channel 2 GPO2 configuration.<br>0 = (Default) Disabled<br>1 = Enabled |
| 0 | IN2_GPO1_SEL | Input Channel 2 GPO1 configuration.<br>0 = (Default) Disabled<br>1 = Enabled |

## 7.4.25 IN1_BIT_PATT_0

**Address: 0x0000 2220**

| RW | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | IN1_BIT_PATT_0 | | | | | | | | | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15:0 | IN1_BIT_PATT_0 | Input Channel 1 SPI bit pattern for external gain control, bits 17-32. Only used if the bit pattern is longer than 16 bits.<br>The contents of the bit pattern must be left-aligned such that the first bit for transmission is in the MSB. If the bit pattern is shorter than 32 bits, one or more of the LSBs is unused. |

## 7.4.26 IN1_BIT_PATT_1

**Address: 0x0000 2222**

| RW | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | IN1_BIT_PATT_1 | | | | | | | | | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15:0 | IN1_BIT_PATT_1 | Input Channel 1 SPI bit pattern for external gain control, bits 1-16.<br>The contents of the bit pattern must be left-aligned such that the first bit for transmission is in the MSB. If the bit pattern is shorter than 16 bits, one or more of the LSBs is unused.<br>If the external gain is controlled using GPIOs, the GPIO1-4 output logic levels are determined by bits 12–15 respectively. |

## 7.4.27 IN1_EXT_GAIN

**Address: 0x0000 2224**

| RW | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | — | | | | | IN1_EXT_ANA_GAIN | | | | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15:11 | — | Reserved |
| 10:0 | IN1_EXT_ANA_GAIN | Input Channel 1 external analog gain. The selected value must match the external analog gain of the associated SPI bit pattern.<br>0x000 = (Default) 0.000 dB<br>0x001 = 0.125 dB<br>0x002 = 0.250 dB<br>…<br>0x23F = 71.875 dB<br>0x240–0x5BF = Reserved<br>0x5C0 = –72.000 dB<br>…<br>0x7FF = –0.125 dB |


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## 7.4.28 IN1_INT_GAIN

**Address: 0x0000 2226**

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | IN1_UPDATE | — | IN1_INT_ANA_GAIN | | — | | | IN1_INT_DIG_GAIN | | | | | | | | |
| Access | WO | — | RW | | — | | | RW | | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15 | IN1_UPDATE | Input Channel 1 gain update. Write 1 to apply the Channel 1 gain selection and SPI bit pattern. The gain update is applied at the next scheduling opportunity, zero-cross aligned. |
| 14 | — | Reserved |
| 13:12 | IN1_INT_ANA_GAIN | Input Channel 1 internal analog gain.<br>00 = (Default) 0 dB<br>01 = 6 dB<br>10 = Reserved<br>11 = 12 dB |
| 11:9 | — | Reserved |
| 8:0 | IN1_INT_DIG_GAIN | Input Channel 1 digital gain. Note the signal level is also controlled by the digital volume.<br>0x000 = (Default) 0.000 dB<br>0x001 = 0.125 dB<br>…<br>0x0FF = 31.875 dB<br>0x100 = –32.000 dB<br>…<br>0x1FF = –0.125 dB |

## 7.4.29 IN2_BIT_PATT_0

**Address: 0x0000 2228**

| RW | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | IN2_BIT_PATT_0 | | | | | | | | | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15:0 | IN2_BIT_PATT_0 | Input Channel 2 SPI bit pattern for external gain control, bits 17-32. Only used if the bit pattern is longer than 16 bits.<br>The contents of the bit pattern must be left-aligned such that the first bit for transmission is in the MSB. If the bit pattern is shorter than 32 bits, one or more of the LSBs is unused. |

## 7.4.30 IN2_BIT_PATT_1

**Address: 0x0000 222A**

| RW | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | IN2_BIT_PATT_1 | | | | | | | | | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15:0 | IN2_BIT_PATT_1 | Input Channel 2 SPI bit pattern for external gain control, bits 1-16.<br>The contents of the bit pattern must be left-aligned such that the first bit for transmission is in the MSB. If the bit pattern is shorter than 16 bits, one or more of the LSBs is unused.<br>If the external gain is controlled using GPIOs, the GPIO1-4 output logic levels are determined by bits 12–15 respectively. |

## 7.4.31 IN2_EXT_GAIN

**Address: 0x0000 222C**

| RW | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | — | | | | | IN2_EXT_ANA_GAIN | | | | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15:11 | — | Reserved |
| 10:0 | IN2_EXT_ANA_GAIN | Input Channel 2 external analog gain. The selected value must match the external analog gain of the associated SPI bit pattern.<br>0x000 = (Default) 0.000 dB<br>0x001 = 0.125 dB<br>…<br>0x23F = 71.875 dB<br>0x240–0x5BF = Reserved<br>0x5C0 = –72.000 dB<br>…<br>0x7FF = –0.125 dB |


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## 7.4.32 IN2_INT_GAIN

**Address: 0x0000 222E**

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | IN2_UPDATE | — | IN2_INT_ANA_GAIN | | — | | | IN2_INT_DIG_GAIN | | | | | | | | |
| Access | WO | — | RW | | — | | | RW | | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15 | IN2_UPDATE | Input Channel 2 gain update. Write 1 to apply the Channel 2 gain selection and SPI bit pattern. The gain update is applied at the next scheduling opportunity, zero-cross aligned. |
| 14 | — | Reserved |
| 13:12 | IN2_INT_ANA_GAIN | Input Channel 2 internal analog gain.<br>00 = (Default) 0 dB<br>01 = 6 dB<br>10 = Reserved<br>11 = 12 dB |
| 11:9 | — | Reserved |
| 8:0 | IN2_INT_DIG_GAIN | Input Channel 2 digital gain. Note that the signal level is also controlled by the digital volume.<br>0x000 = (Default) 0.000 dB<br>0x001 = 0.125 dB<br>…<br>0x0FF = 31.875 dB<br>0x100 = –32.000 dB<br>…<br>0x1FF = –0.125 dB |

## 7.4.33 IN1_LOW_BIT_PATT_0

**Address: 0x0000 2260**

| RW | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | IN1_LOW_BIT_PATT_0 | | | | | | | | | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15:0 | IN1_LOW_BIT_PATT_0 | Input Channel 1 SPI bit pattern for external gain control,low gain setting for PAD on, bits 17-32. Only used if the bit pattern is longer than 16 bits.<br>The contents of the bit pattern must be left-aligned such that the first bit for transmission is in the MSB. If the bit pattern is shorter than 32 bits, one or more of the LSBs is unused. |

## 7.4.34 IN1_LOW_BIT_PATT_1

**Address: 0x0000 2262**

| RW | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | IN1_LOW_BIT_PATT_1 | | | | | | | | | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15:0 | IN1_LOW_BIT_PATT_1 | Input Channel 1 SPI bit pattern for external gain control, bits 1-16.<br>The contents of the bit pattern must be left-aligned such that the first bit for transmission is in the MSB. If the bit pattern is shorter than 16 bits, one or more of the LSBs is unused.<br>If the external gain is controlled using GPIOs, the GPIO1-4 output logic levels are determined by bits 12–15 respectively. |

## 7.4.35 IN1_LOW_EXT_GAIN

**Address: 0x0000 2264**

| RW | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | — | | | | | IN1_LOW_EXT_ANA_GAIN | | | | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15:11 | — | Reserved |
| 10:0 | IN1_LOW_EXT_ANA_GAIN | Input Channel 1 external analog gain. The selected value must match the analog gain of the associated SPI bit pattern.<br>0x000 = (Default) 0.000 dB<br>0x001 = 0.125 dB<br>…<br>0x23F = 71.875 dB<br>0x240–0x5BF = Reserved<br>0x5C0 = –72.000 dB<br>…<br>0x7FF = –0.125 dB |


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## 7.4.36 IN1_LOW_INT_GAIN

**Address: 0x0000 2266**

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | IN1_LOW_UPDATE | — | IN1_LOW_INT_ANA_GAIN | | — | | | IN1_LOW_INT_DIG_GAIN | | | | | | | | |
| Access | WO | — | RW | | — | | | RW | | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15 | IN1_LOW_UPDATE | Input Channel 1 gain update. Write 1 to apply the Channel 1 gain selection and SPI bit pattern. The gain update is applied at the next scheduling opportunity, zero-cross aligned. |
| 14 | — | Reserved |
| 13:12 | IN1_LOW_INT_ANA_GAIN | Input Channel 1 internal analog gain.<br>00 = (Default) 0 dB<br>01 = 6 dB<br>10 = Reserved<br>11 = 12 dB |
| 11:9 | — | Reserved |
| 8:0 | IN1_LOW_INT_DIG_GAIN | Input Channel 1 digital gain.<br>0x000 = (Default) 0.000 dB<br>0x001 = 0.125 dB<br>…<br>0x0FF = 31.875 dB<br>0x100 = –32.000 dB<br>…<br>0x1FF = –0.125 dB |

## 7.4.37 IN2_LOW_BIT_PATT_0

**Address: 0x0000 2268**

| RW | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | IN2_LOW_BIT_PATT_0 | | | | | | | | | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15:0 | IN2_LOW_BIT_PATT_0 | Input Channel 2 SPI bit pattern for external gain control, low gain setting for PAD on, bits 17-32. Only used if the bit pattern is longer than 16 bits.<br>The contents of the bit pattern must be left-aligned such that the first bit for transmission is in the MSB. If the bit pattern is shorter than 32 bits, one or more of the LSBs is unused. |

## 7.4.38 IN2_LOW_BIT_PATT_1

**Address: 0x0000 226A**

| RW | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | IN2_LOW_BIT_PATT_1 | | | | | | | | | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15:0 | IN2_LOW_BIT_PATT_1 | Input Channel 2 SPI bit pattern for external gain control, bits 1-16.<br>The contents of the bit pattern must be left-aligned such that the first bit for transmission is in the MSB. If the bit pattern is shorter than 16 bits, one or more of the LSBs is unused.<br>If the external gain is controlled using GPIOs, the GPIO1-4 output logic levels are determined by bits 12–15 respectively. |

## 7.4.39 IN2_LOW_EXT_GAIN

**Address: 0x0000 226C**

| RW | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | — | | | | | IN2_LOW_EXT_ANA_GAIN | | | | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15:11 | — | Reserved |
| 10:0 | IN2_LOW_EXT_ANA_GAIN | Input Channel 2 external analog gain. The selected value must match the analog gain of the associated SPI bit pattern.<br>0x000 = (Default) 0.000 dB<br>0x001 = 0.125 dB<br>…<br>0x23F = 71.875 dB<br>0x240–0x5BF = Reserved<br>0x5C0 = –72.000 dB<br>…<br>0x7FF = –0.125 dB |


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## 7.4.40 IN2_LOW_INT_GAIN

**Address: 0x0000 226E**

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | IN2_LOW_UPDATE | — | IN2_LOW_INT_ANA_GAIN | | — | | | | IN2_LOW_INT_DIG_GAIN | | | | | | | |
| Access | WO | — | RW | | — | | | | RW | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15 | IN2_LOW_UPDATE | Input Channel 2 gain update. Write 1 to apply Channel 2 gain selection and SPI bit pattern. The gain update is applied at the next scheduling opportunity, zero-cross aligned. |
| 14 | — | Reserved |
| 13:12 | IN2_LOW_INT_ANA_GAIN | Input Channel 2 internal analog gain.<br>00 = (Default) 0 dB<br>01 = 6 dB<br>10 = Reserved<br>11 = 12 dB |
| 11:9 | — | Reserved |
| 8:0 | IN2_LOW_INT_DIG_GAIN | Input Channel 2 digital gain.<br>0x000 = (Default) 0.000 dB<br>0x001 = 0.125 dB<br>…<br>0x0FF = 31.875 dB<br>0x100 = –32.000 dB<br>…<br>0x1FF = –0.125 dB |

## 7.4.41 IN1_HIGH_BIT_PATT_0

**Address: 0x0000 22C0**

| RW | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | IN1_HIGH_BIT_PATT_0 | | | | | | | | | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15:0 | IN1_HIGH_BIT_PATT_0 | Input Channel 1 SPI bit pattern for external gain control, high gain setting for PAD off, bits 17-32. Only used if the bit pattern is longer than 16 bits.<br>The contents of the bit pattern must be left-aligned such that the first bit for transmission is in the MSB. If the bit pattern is shorter than 32 bits, one or more of the LSBs is unused. |

## 7.4.42 IN1_HIGH_BIT_PATT_1

**Address: 0x0000 22C2**

| RW | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | IN1_HIGH_BIT_PATT_1 | | | | | | | | | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15:0 | IN1_HIGH_BIT_PATT_1 | Input Channel 1 SPI bit pattern for external gain control, bits 1-16.<br>The contents of the bit pattern must be left-aligned such that the first bit for transmission is in the MSB. If the bit pattern is shorter than 16 bits, one or more of the LSBs is unused.<br>If the external gain is controlled using GPIOs, the GPIO1-4 output logic levels are determined by bits 12–15 respectively. |

## 7.4.43 IN1_HIGH_EXT_GAIN

**Address: 0x0000 22C4**

| RW | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | — | | | | | IN1_HIGH_EXT_ANA_GAIN | | | | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15:11 | — | Reserved |
| 10:0 | IN1_HIGH_EXT_ANA_GAIN | Input Channel 1 external analog gain. The selected value must match the analog gain of the associated SPI bit pattern.<br>0x000 = (Default) 0.000 dB<br>0x001 = 0.125 dB<br>0x002 = 0.250 dB<br>…<br>0x23F = 71.875 dB<br>0x240–0x5BF = Reserved<br>0x5C0 = –72.000 dB<br>…<br>0x7FF = –0.125 dB |


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## 7.4.44 IN1_HIGH_INT_GAIN

**Address: 0x0000 22C6**

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | IN1_HIGH_UPDATE | — | IN1_HIGH_INT_ANA_GAIN | | — | | | | IN1_HIGH_INT_DIG_GAIN | | | | | | | |
| Access | WO | — | RW | | — | | | | RW | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15 | IN1_HIGH_UPDATE | Input Channel 1 gain update. Write 1 to apply the Channel 1 gain selection and SPI bit pattern. The gain update is applied at the next scheduling opportunity, zero-cross aligned. |
| 14 | — | Reserved |
| 13:12 | IN1_HIGH_INT_ANA_GAIN | Input Channel 1 internal analog gain.<br>00 = (Default) 0 dB<br>01 = 6 dB<br>10 = Reserved<br>11 = 12 dB |
| 11:9 | — | Reserved |
| 8:0 | IN1_HIGH_INT_DIG_GAIN | Input Channel 1 digital gain.<br>0x000 = (Default) 0.000 dB<br>0x001 = 0.125 dB<br>…<br>0x0FF = 31.875 dB<br>0x100 = –32.000 dB<br>…<br>0x1FF = –0.125 dB |

## 7.4.45 IN2_HIGH_BIT_PATT_0

**Address: 0x0000 22C8**

| RW | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | IN2_HIGH_BIT_PATT_0 | | | | | | | | | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15:0 | IN2_HIGH_BIT_PATT_0 | Input Channel 2 SPI bit pattern for external gain control, high gain setting for PAD off, bits 17-32. Only used if the bit pattern is longer than 16 bits.<br>The contents of the bit pattern must be left-aligned such that the first bit for transmission is in the MSB. If the bit pattern is shorter than 32 bits, one or more of the LSBs is unused. |

## 7.4.46 IN2_HIGH_BIT_PATT_1

**Address: 0x0000 22CA**

| RW | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | IN2_HIGH_BIT_PATT_1 | | | | | | | | | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15:0 | IN2_HIGH_BIT_PATT_1 | Input Channel 2 SPI bit pattern for external gain control, bits 1-16.<br>The contents of the bit pattern must be left-aligned such that the first bit for transmission is in the MSB. If the bit pattern is shorter than 16 bits, one or more of the LSBs is unused.<br>If the external gain is controlled using GPIOs, the GPIO1-4 output logic levels are determined by bits 12–15 respectively. |

## 7.4.47 IN2_HIGH_EXT_GAIN

**Address: 0x0000 22CC**

| RW | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | — | | | | | IN2_HIGH_EXT_ANA_GAIN | | | | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15:11 | — | Reserved |
| 10:0 | IN2_HIGH_EXT_ANA_GAIN | Input Channel 2 external analog gain. The selected value must match the analog gain of the associated SPI bit pattern.<br>0x000 = (Default) 0.000 dB<br>0x001 = 0.125 dB<br>…<br>0x23F = 71.875 dB<br>0x240–0x5BF = Reserved<br>0x5C0 = –72.000 dB<br>…<br>0x7FF = –0.125 dB |


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## 7.4.48 IN2_HIGH_INT_GAIN

**Address: 0x0000 22CE**

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | IN2_HIGH_UPDATE | — | IN2_HIGH_INT_ANA_GAIN | | — | | | | IN2_HIGH_INT_DIG_GAIN | | | | | | | |
| Access | WO | — | RW | | — | | | | RW | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15 | IN2_HIGH_UPDATE | Input Channel 2 gain update. Write 1 to apply the Channel 2 gain selection and SPI bit pattern. The gain update is applied at the next scheduling opportunity, zero-cross aligned. |
| 14 | — | Reserved |
| 13:12 | IN2_HIGH_INT_ANA_GAIN | Input Channel 2 internal analog gain.<br>00 = (Default) 0 dB<br>01 = 6 dB<br>10 = Reserved<br>11 = 12 dB |
| 11:9 | — | Reserved |
| 8:0 | IN2_HIGH_INT_DIG_GAIN | Input Channel 2 digital gain.<br>0x000 = (Default) 0.000 dB<br>0x001 = 0.125 dB<br>…<br>0x0FF = 31.875 dB<br>0x100 = –32.000 dB<br>…<br>0x1FF = –0.125 dB |

## 7.4.49 AUX1_CFG

**Address: 0x0000 2900**

| RW | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | — | | | | | AUX1_SPI_POSITION | | | — | | AUX1_BIT_PATT_LENGTH | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15:11 | — | Reserved |
| 10:8 | AUX1_SPI_POSITION | AUX Device 1 position in the SPI chain. |
| 7:6 | — | Reserved |
| 5:0 | AUX1_BIT_PATT_LENGTH | AUX Device 1 bit-pattern length for SPI AUX control.<br>0x00 = (Default) 0 bits (device not present)<br>0x01 = 1 bits<br>0x02 = 2 bits<br>…<br>0x20 = 32 bits<br>0x21–0x3F = Reserved |

## 7.4.50 AUX2_CFG

**Address: 0x0000 2904**

| RW | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | — | | | | | AUX2_SPI_POSITION | | | — | | AUX2_BIT_PATT_LENGTH | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15:11 | — | Reserved |
| 10:8 | AUX2_SPI_POSITION | AUX Device 2 position in the SPI chain. |
| 7:6 | — | Reserved |
| 5:0 | AUX2_BIT_PATT_LENGTH | AUX Device 2 bit-pattern length for SPI AUX control.<br>0x00 = (Default) 0 bits (device not present)<br>0x01 = 1 bits<br>0x02 = 2 bits<br>…<br>0x20 = 32 bits<br>0x21–0x3F = Reserved |


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### 7.4.51 AUX1_BIT_PATT_0

**Address: 0x0000 2920**

| RW | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | AUX1_BIT_PATT_0 | | | | | | | | | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15:0 | AUX1_BIT_PATT_0 | AUX Device 1 SPI bit pattern, bits 17-32. Only used if the bit pattern is longer than 16 bits.<br>The contents of the bit pattern must be left-aligned such that the first bit for transmission is in the MSB. If the bit pattern is shorter than 32 bits, one or more of the LSBs is unused. |

### 7.4.52 AUX1_BIT_PATT_1

**Address: 0x0000 2922**

| RW | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | AUX1_BIT_PATT_1 | | | | | | | | | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15:0 | AUX1_BIT_PATT_1 | AUX Device 1 SPI bit pattern, bits 1-16.<br>The contents of the bit pattern must be left-aligned such that the first bit for transmission is in the MSB. If the bit pattern is shorter than 16 bits, one or more of the LSBs is unused. |

### 7.4.53 AUX2_BIT_PATT_0

**Address: 0x0000 2924**

| RW | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | AUX2_BIT_PATT_0 | | | | | | | | | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15:0 | AUX2_BIT_PATT_0 | AUX Device 2 SPI bit pattern, bits 17-32. Only used if the bit pattern is longer than 16 bits.<br>The contents of the bit pattern must be left-aligned such that the first bit for transmission is in the MSB. If the bit pattern is shorter than 32 bits, one or more of the LSBs is unused. |

### 7.4.54 AUX2_BIT_PATT_1

**Address: 0x0000 2926**

| RW | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | AUX2_BIT_PATT_1 | | | | | | | | | | | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15:0 | AUX2_BIT_PATT_1 | AUX Device 2 SPI bit pattern, bits 1-16.<br>The contents of the bit pattern must be left-aligned such that the first bit for transmission is in the MSB. If the bit pattern is shorter than 16 bits, one or more of the LSBs is unused. |

## 7.5 PIN_CONFIG

### 7.5.1 PAD_IRQ_CFG

**Address: 0x0000 3D1C**

| RW | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | IRQ_OP_CFG | — | | | | | | GPIO1_IRQ_EN | GPIO2_IRQ_EN | — | | CONFIG4_IRQ_EN | SPI_SCK_IRQ_EN | — | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15 | IRQ_OP_CFG | IRQ output configuration<br>0 = (Default) CMOS<br>1 = Open drain |
| 14:9 | — | Reserved |
| 8 | GPIO1_IRQ_EN | IRQ output to GPIO1<br>0 = (Default) GPIO1<br>1 = IRQ output |


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| Bits | Name | Description |
|---|---|---|
| 7 | GPIO2_IRQ_EN | IRQ output to GPIO2<br>0 = (Default) GPIO2<br>1 = IRQ output |
| 6:5 | — | Reserved |
| 4 | CONFIG4_IRQ_EN | CONFIG4 pin function select<br>0 = (Default) HW config/CH_IDLE<br>1 = IRQ output |
| 3 | SPI_SCK_IRQ_EN | IRQ output to SPI_SCK<br>0 = (Default) SPI_SCK<br>1 = IRQ output |
| 2:0 | — | Reserved |

## 7.6 IRQ_CONFIG

### 7.6.1 IRQ_STS

**Address: 0x0000 3E04**

| RO | 15…8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| | — | — | | | | | | | IRQ_STS |
| Default | 0x00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15:1 | — | Reserved |
| 0 | IRQ_STS | IRQ status. Logical OR of all unmasked x_INT interrupts.<br>0 = (Default) Not asserted<br>1 = Asserted |

### 7.6.2 IRQ_ADC_EVENT_INT

**Address: 0x0000 3E1C**

| RW | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | — | | | | IN2_PAD_LOW_INT | IN1_PAD_LOW_INT | IN2_PAD_HIGH_INT | IN1_PAD_HIGH_INT | GAIN_CONFLICT_INT | — | | | | IN2_CLIP_WARN_INT | IN1_CLIP_WARN_INT | — |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15:12 | — | Reserved |
| 11 | IN2_PAD_LOW_INT | ADC Channel 2 PAD LD, input signal exceeds low-level threshold interrupt. Write 1 to clear.<br>0 = (Default) Normal<br>1 = Exceeds Low Th |
| 10 | IN1_PAD_LOW_INT | ADC Channel 1 PAD LD, input signal exceeds low-level threshold interrupt. Write 1 to clear.<br>0 = (Default) Normal<br>1 = Exceeds Low Th |
| 9 | IN2_PAD_HIGH_INT | ADC Channel 2 PAD LD, input signal exceeds high-level threshold interrupt. Write 1 to clear.<br>0 = (Default) Normal<br>1 = Exceed High Th |
| 8 | IN1_PAD_HIGH_INT | ADC Channel 1 PAD LD, input signal exceeds high-level threshold interrupt. Write 1 to clear.<br>0 = (Default) Normal<br>1 = Exceed High Th |
| 7 | GAIN_CONFLICT_INT | Gain updates both high gain and low gain concurrently interrupt. Write 1 to clear.<br>0 = (Default) Normal<br>1 = Update conflict |
| 6:3 | — | Reserved |
| 2 | IN2_CLIP_WARN_INT | Channel 2 clip-detect warning interrupt, rising-edge triggered. Write 1 to clear.<br>0 = (Default) Normal<br>1 = Clip detect |
| 1 | IN1_CLIP_WARN_INT | Channel 1 clip-detect warning interrupt, rising-edge triggered. Write 1 to clear.<br>0 = (Default) Normal<br>1 = Clip detect |
| 0 | — | Reserved |


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### 7.6.3 IRQ_HGC_EVENT_INT

**Address: 0x0000 3E1E**

| RW | 15…8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| | — | — | | | HGC_SPI_ERROR_INT | HGC_ABORT_ERROR_INT | — | HGC_ERROR_INT | HGC_DONE_INT |
| Default | 0x00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15:5 | — | Reserved |
| 4 | HGC_SPI_ERROR_INT | HGC Gain update SPI error interrupt. Write 1 to clear.<br>0 = (Default) Normal<br>1 = HGC update SPI error |
| 3 | HGC_ABORT_ERROR_INT | HGC Gain update aborted interrupt. Write 1 to clear.<br>0 = (Default) Normal<br>1 = HGC update aborted |
| 2 | — | Reserved |
| 1 | HGC_ERROR_INT | HGC Gain updates failed interrupt. Write 1 to clear.<br>0 = (Default) Normal<br>1 = HGC update failed |
| 0 | HGC_DONE_INT | HGC Gain updates have completed successfully interrupt, rising-edge triggered. Write 1 to clear.<br>0 = (Default) Normal<br>1 = HGC gain changed |

### 7.6.4 IRQ_ADC_EVENT_MASK

**Address: 0x0000 3E2C**

| RW | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | — | | | | IN2_PAD_LOW_MASK | IN1_PAD_LOW_MASK | IN2_PAD_HIGH_MASK | IN1_PAD_HIGH_MASK | GAIN_CONFLICT_MASK | — | | | | IN2_CLIP_WARN_MASK | IN1_CLIP_WARN_MASK | — |
| Default | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15:12 | — | Reserved |
| 11 | IN2_PAD_LOW_MASK | ADC Channel 2 PAD LD, input signal exceeds low-level threshold interrupt mask.<br>0 = Do Not Mask<br>1 = (Default) Mask Interrupt |
| 10 | IN1_PAD_LOW_MASK | ADC Channel 1 PAD LD, input signal exceeds low-level threshold interrupt mask.<br>0 = Do Not Mask<br>1 = (Default) Mask Interrupt |
| 9 | IN2_PAD_HIGH_MASK | ADC Channel 2 PAD LD, input signal exceeds high-level threshold interrupt mask.<br>0 = Do Not Mask<br>1 = (Default) Mask Interrupt |
| 8 | IN1_PAD_HIGH_MASK | ADC Channel 1 PAD LD, input signal exceeds high-level threshold interrupt mask.<br>0 = Do Not Mask<br>1 = (Default) Mask Interrupt |
| 7 | GAIN_CONFLICT_MASK | Gain updates both high gain and low gain interrupt mask.<br>0 = Do Not Mask<br>1 = (Default) Mask Interrupt |
| 6:3 | — | Reserved |
| 2 | IN2_CLIP_WARN_MASK | ADC Channel 2 clip-detect warning interrupt mask.<br>0 = (Default) Do Not Mask<br>1 = Mask Interrupt |
| 1 | IN1_CLIP_WARN_MASK | ADC Channel 1 clip-detect warning interrupt mask.<br>0 = (Default) Do Not Mask<br>1 = Mask Interrupt |
| 0 | — | Reserved |


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## 7.6.5 IRQ_HGC_EVENT_MASK

**Address: 0x0000 3E2E**

| RW | 15…8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|
| | — | — | | | HGC_SPI_ERROR_MASK | HGC_ABORT_MASK | — | HGC_ERROR_MASK | HGC_DONE_MASK |
| Default | 0x00 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |

| Bits | Name | Description |
|---|---|---|
| 15:5 | — | Reserved |
| 4 | HGC_SPI_ERROR_MASK | HGC Gain update SPI error interrupt mask.<br>0 = Do Not Mask<br>1 = (Default) Mask Interrupt |
| 3 | HGC_ABORT_MASK | HGC Gain update aborted interrupt mask.<br>0 = Do Not Mask<br>1 = (Default) Mask Interrupt |
| 2 | — | Reserved |
| 1 | HGC_ERROR_MASK | HGC Gain updates failed interrupt mask.<br>0 = Do Not Mask<br>1 = (Default) Mask Interrupt |
| 0 | HGC_DONE_MASK | HGC Gain updates have completed interrupt mask.<br>0 = Do Not Mask<br>1 = (Default) Mask Interrupt |

## 7.6.6 IRQ_ADC_EVENT_STS

**Address: 0x0000 3E5C**

| RO | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | — | | | | IN2_PAD_LOW_STS | IN1_PAD_LOW_STS | IN2_PAD_HIGH_STS | IN1_PAD_HIGH_STS | — | | | | | IN2_CLIP_WARN_STS | IN1_CLIP_WARN_STS | — |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 15:12 | — | Reserved |
| 11 | IN2_PAD_LOW_STS | ADC Channel 2 PAD LD, input signal exceeds low-level threshold status.<br>0 = (Default) Not asserted<br>1 = Asserted |
| 10 | IN1_PAD_LOW_STS | ADC Channel 1 PAD LD, input signal exceeds low-level threshold status.<br>0 = (Default) Not asserted<br>1 = Asserted |
| 9 | IN2_PAD_HIGH_STS | ADC Channel 2 PAD LD, input signal exceeds high-level threshold status.<br>0 = (Default) Not asserted<br>1 = Asserted |
| 8 | IN1_PAD_HIGH_STS | ADC Channel 1 PAD LD, input signal exceeds high-level threshold status.<br>0 = (Default) Not asserted<br>1 = Asserted |
| 7:3 | — | Reserved |
| 2 | IN2_CLIP_WARN_STS | ADC Channel 2 clip warning status.<br>0 = (Default) Not asserted<br>1 = Asserted |
| 1 | IN1_CLIP_WARN_STS | ADC Channel 1 clip warning status.<br>0 = (Default) Not asserted<br>1 = Asserted |
| 0 | — | Reserved |


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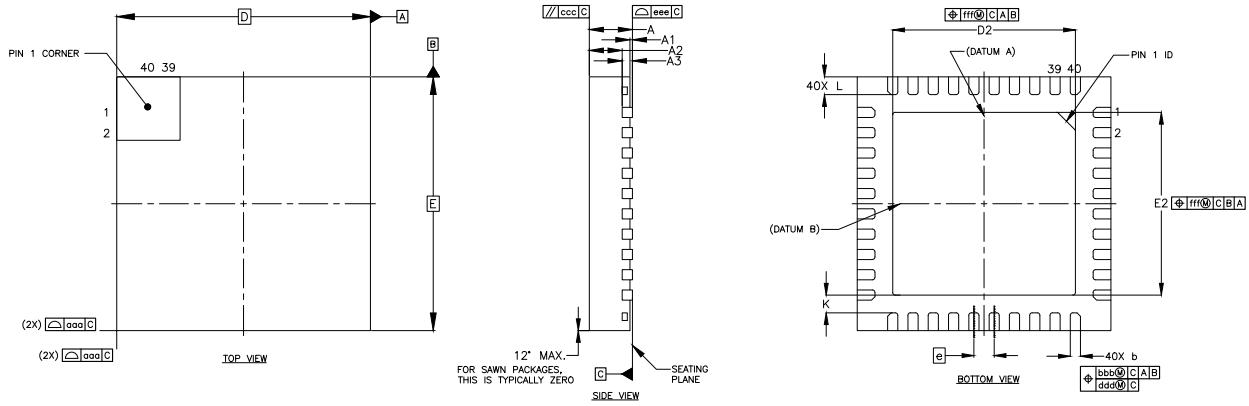
# 8 Thermal Characteristic

**Table 8-1. Typical JEDEC Four-Layer, 2s2p Board Thermal Characteristics**

| Parameter | Symbol | QFN | Units |
|---|---|---|---|
| Junction-to-ambient thermal resistance | $\theta_{JA}$ | 29.62 | °C/W |
| Junction-to-board thermal resistance | $\theta_{JB}$ | 16.37 | °C/W |
| Junction-to-case (top) thermal resistance | $\theta_{JC}$ | 54.85 | °C/W |
| Junction-to-board thermal-characterization parameter | $\Psi_{JB}$ | 15.21 | °C/W |
| Junction-to-package-top thermal-characterization parameter | $\Psi_{JT}$ | 2.38 | °C/W |

**Notes:**
- Natural convection at the maximum recommended operating temperature $T_A$ (see Table 3-2)
- Four-layer, 2s2p PCB as specified by JESD51–9 and JESD51–11; dimensions: 101.5 x 114.5 x 1.6 mm
- Thermal parameters as defined by JESD51–12

# 9 Package Dimensions




| | | SYMBOL | MIN | NOM | MAX |
|---|---|---|---|---|---|
| TOTAL THICKNESS | | A | 0.80 | 0.85 | 0.90 |
| STAND OFF | | A1 | 0 | 0.02 | 0.05 |
| MOLD THICKNESS | | A2 | – | 0.65 | – |
| L/F THICKNESS | | A3 | 0.20 REF. | | |
| LEAD WIDTH | | b | 0.15 | 0.20 | 0.25 |
| BODY SIZE | X | D | 5.0 BSC | | |
| | Y | E | 5.0 BSC | | |
| LEAD PITCH | | e | 0.40 BSC | | |
| EP SIZE | X | D2 | 3.50 | 3.60 | 3.70 |
| | Y | E2 | 3.50 | 3.60 | 3.70 |
| LEAD LENGTH | | L | 0.30 | 0.35 | 0.40 |
| LEAD TO EP CLEARANCE | | K | 0.35 REF. | | |
| PACKAGE EDGE TOLERANCE | | aaa | 0.10 | | |
| LEAD OFFSET | | bbb | 0.07 | | |
| | | ddd | 0.05 | | |
| MOLD FLATNESS | | ccc | 0.10 | | |
| COPLANARITY | | eee | 0.08 | | |
| EXPOSED PAD OFFSET | | fff | 0.10 | | |

**Figure 9-1. QFN Package Drawing**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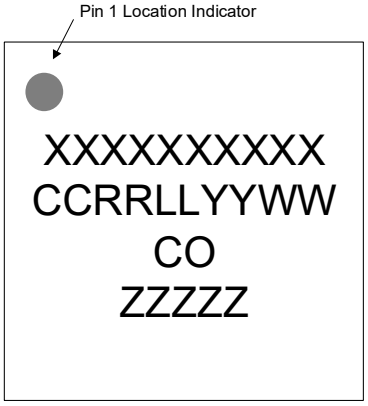
# 10 Package Marking

**Figure 10-1. Package Marking**




**Top Side Brand**
Line 1: Part number
Line 2: Package mark
Line 3: Country of origin (CO)
Line 4: Encoded wafer/device ID

**Package Mark Fields**
CC = Cirrus Logic Index Code
RR = Device revision code
LL = Lot sequence code
YY = Year of manufacture
WW = Work week of manufacture

# 11 Ordering Information

**Table 11-1. Ordering Information**

| Product | Description | Package | Environmental Certifications | Grade | Temperature Range | Container | Orderable Part Number |
|---|---|---|---|---|---|---|---|
| CS5312S | High Performance Two-Channel Audio ADC | 40-pin QFN | RoHS Compliant | Commercial | –40 to +85°C | Tray | CS5312S-DN |
| | | | | | | Tape and Reel | CS5312S-DNR |

# 12 References

- NXP Semiconductors, UM10204 Rev. 7, October 2021, *I2C-Bus Specification and User Manual*, https://www.nxp.com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# 13 Revision History

**Important:** Please check www.cirrus.com or with your Cirrus Logic sales representative to confirm that you are using the latest revision of this document and to determine whether there are errata associated with this device.

**Table 13-1. Revision History**

| Revision | Change |
|---|---|
| A3<br>OCT 2026 | • Updated Dynamic Range and THD+N values in Specifications.<br>• Updated Pin Assignments and Descriptions (changes reflected throughout) (Section 1):<br>—Renamed Pin 1 was GND_D, now NC; PAD was GND_A, now GND.<br>—Changed LDO_VD_FILT power supply, was VDD_A1 now VDD_A2.<br>—Updated table note related to ground connections<br>• Updated Termination of Unused Pins (Table 1-2).<br>—Removed pin ASP_DOUT.<br>• Updated Typical Connections Diagram (Section 2):<br>—Renamed GND_D, GND_A, and PAD, as summarized above.<br>—Updated decoupling capacitor values on ADC_FILT_x and LDO_VD_FILT pins.<br>—Updated note regarding clocking option configuration.<br>—Added External Component Requirements (Table 2-1).<br>• Updated Characteristics and Specifications (Section 3):<br>—Updated bandwidth condition for performance measurements in Parameter Definitions table note (Table 3-1)<br>—Removed GND_D from test conditions in all tables (Section 3).<br>—Updated table note for Recommended Operating Conditions (Table 3-2).<br>—Added Digital Core (LDO_VD_FILT) to Absolute Maximum Ratings (Table 3-3).<br>—Updated Dynamic Range (A-weighted) and THD_N (0 dBFS) values and table notes in ADC Path Characteristics (Table 3-4).<br>—Updated parameter conditions for Passband ripple and Stopband attenuation for Slow roll-off filter at $F_S$ = 352.8 kHz or 384 kHz in ADC Filter Characteristics (Table 3-5)<br>—Removed Phase Deviation specification in ADC High Pass Filter Characteristics (Table 3-6).<br>—Update test conditions and parameters in Device Power Consumption (Table 3-7).<br>—Removed table note regarding XTAL pin multiplexing in Digital Interface Specifications and Characteristics (Table 3-8).<br>—Removed specification and related note for ADC_FILT maximum output current in DC Characteristics (Table 3-9).<br>—Updated VDD_IO2 POR threshold ($V_{POR}$) rising and falling maximum values in DC Characteristics (Table 3-9).<br>—Removed reference to half-cycle mode in ASP timing in I2S and Left-Justified Modes parameter note in Switching Specifications—Audio Serial Port (ASP) (Table 3-11).<br>—Updated VDD_IO in test conditions in Switching Specifications—SPI Control Port (Table 3-13). |


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**Table 13-1. Revision History *(Cont.)***

| Revision | Change |
|---|---|
| A3<br>OCT 2026 | • Updated Functional Description (Section 4):<br>—Clarified supported sample rates for different system clock frequencies (Section 4.2, Section 4.4, Section 4.4.1, Section 4.4.2, Section 4.9.1, Section 4.9.3).<br>—Clarified external clock synchronization requirements in ASP Secondary Mode (Section 4.4.1, Section 4.4.2, Section 4.9.1).<br>—Corrected debounce time and input polarity configuration availability in Virtual PAD (Section 4.5.5).<br>—Added note in Automatic PAD Response (Section 4.5.5.3).<br>—Corrected operation , including removal of Idle detection in Signal-Activity Detection (Section 4.6).<br>—Updates to field names and function for HGC transient masking in Hybrid Gain Control (Section 4.7).<br>—Edited Gain Ramping Control description in Hybrid Gain Control (Section 4.7)<br>—Updated IRQ Event Logic Output Pins and removed signal-activity detection status in Interrupts (Section 4.11).<br>• Updated Applications (Section 5):<br>—Updated attenuation level for -12 dB/octave slope in Input Buffer Circuit (Section 5.1)<br>—Added PCB Layout Guidelines (Section 5.2).<br>• Edited Registers (Section 7):<br>—MTLREVID<br>—HGC_CTRL_INTERFACE<br>—HGC_CSB_RISE_DLY<br>—HGC_CSB_FALL_DLY<br>—IN_TM_LD_TIME<br>—INx_TM_LD_EN<br>—INx_TM_LD_THR<br>—INx_PAD_LOW_THR<br>—INx_PAD_HIGH_THR<br>—IN_SIG_ACT_HIGH/LOW_EN<br>—INx_SIG_ACT_HIGH/LOW_THR<br>—INx_BIT_PATT_n<br>—INx_LOW/HIGH_BIT_PATT_n<br>—INx_SIG_ACT_LOW/HIGH_INT<br>—INx_SIG_ACT_LOW/HIGH_MASK<br>—INx_SIG_ACT_LOW/HIGH_STS |
| A2<br>MAY 2026 | • Released for public distribution |
| A1<br>NOV 2025 | • Initial version |


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